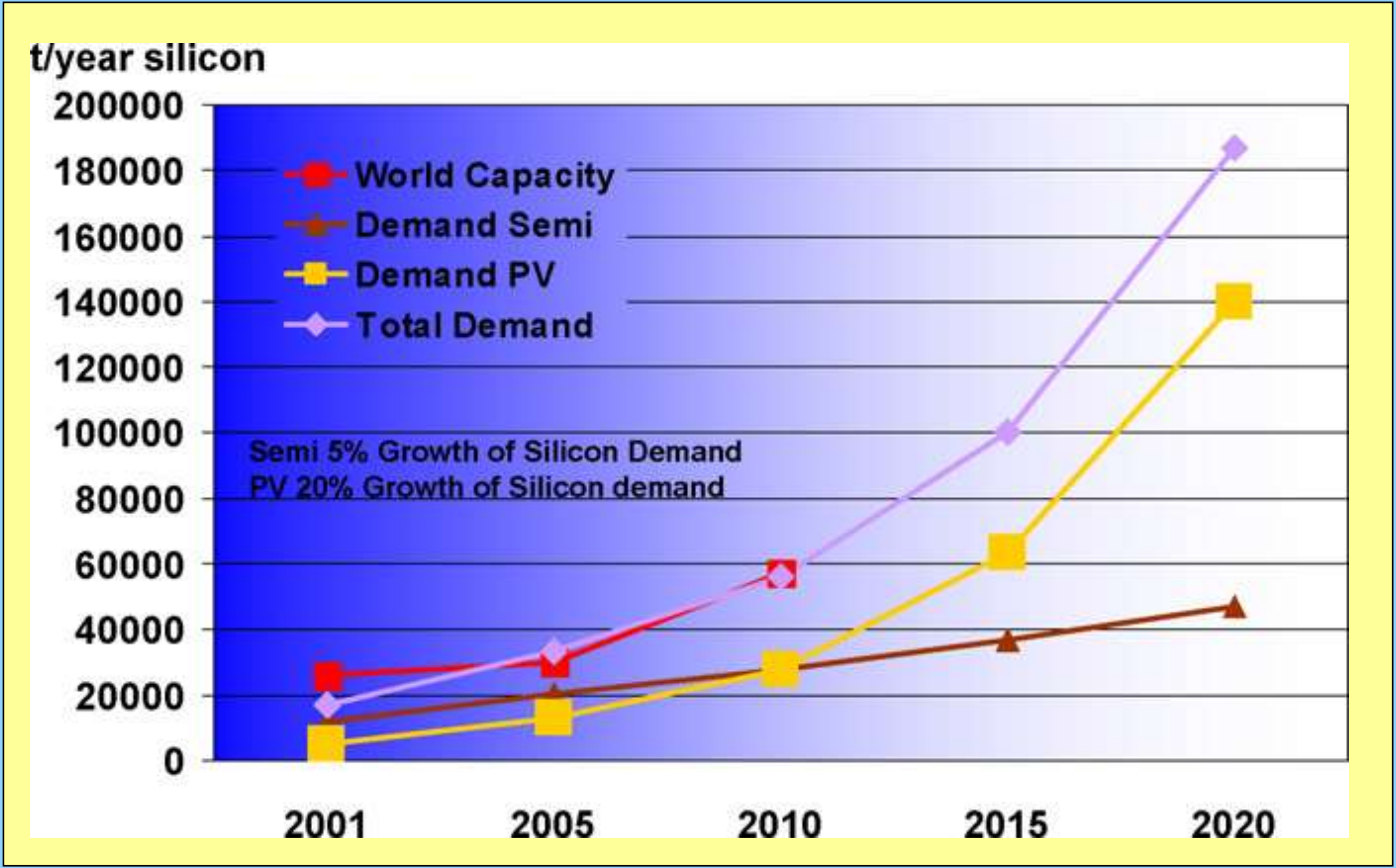
INSTITUTE OF METALLURGY AND MATERIALS SCIENCES

Technology of the solar cells

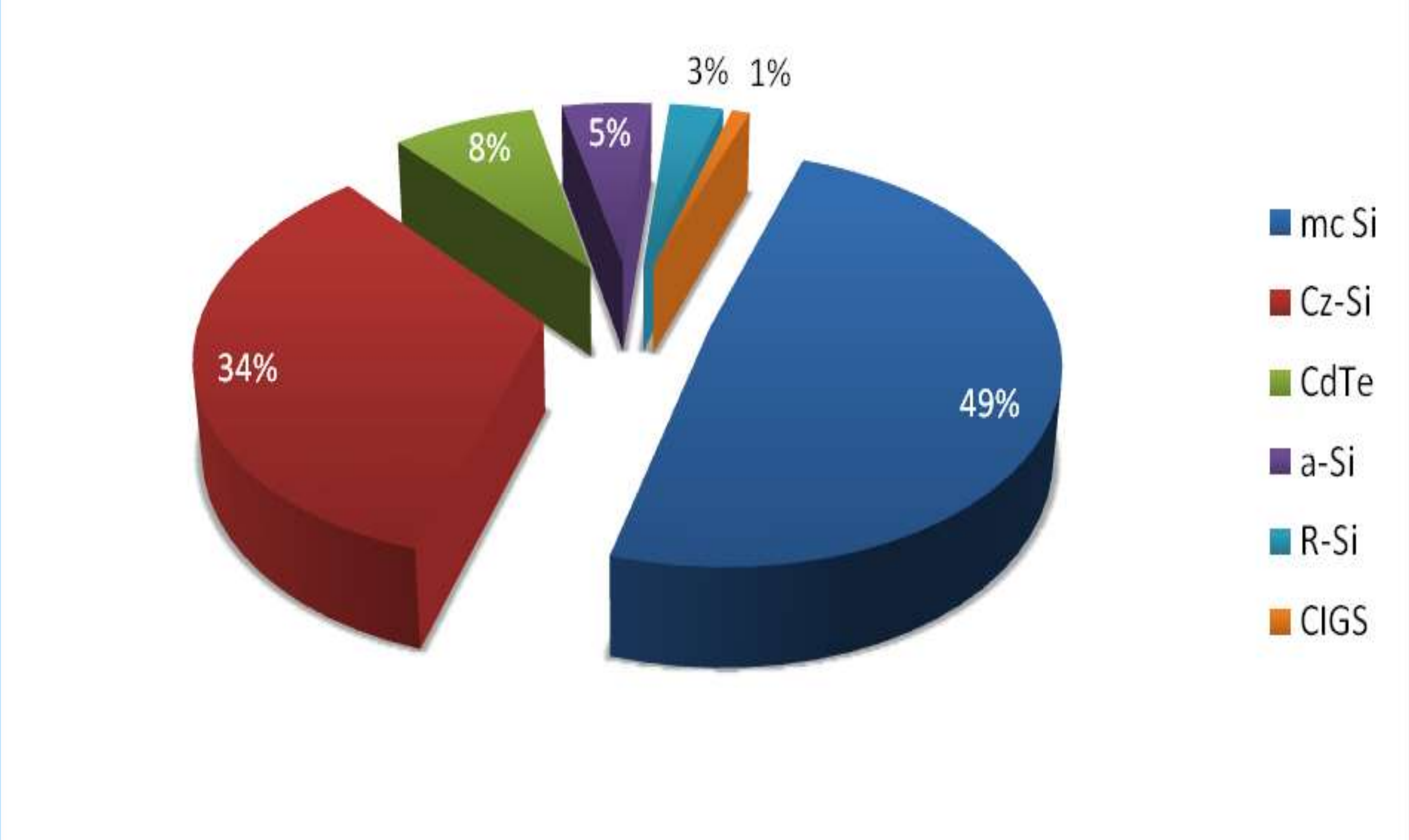
dr Piotr Panek

Future global solar silicon demand (in tonnes)

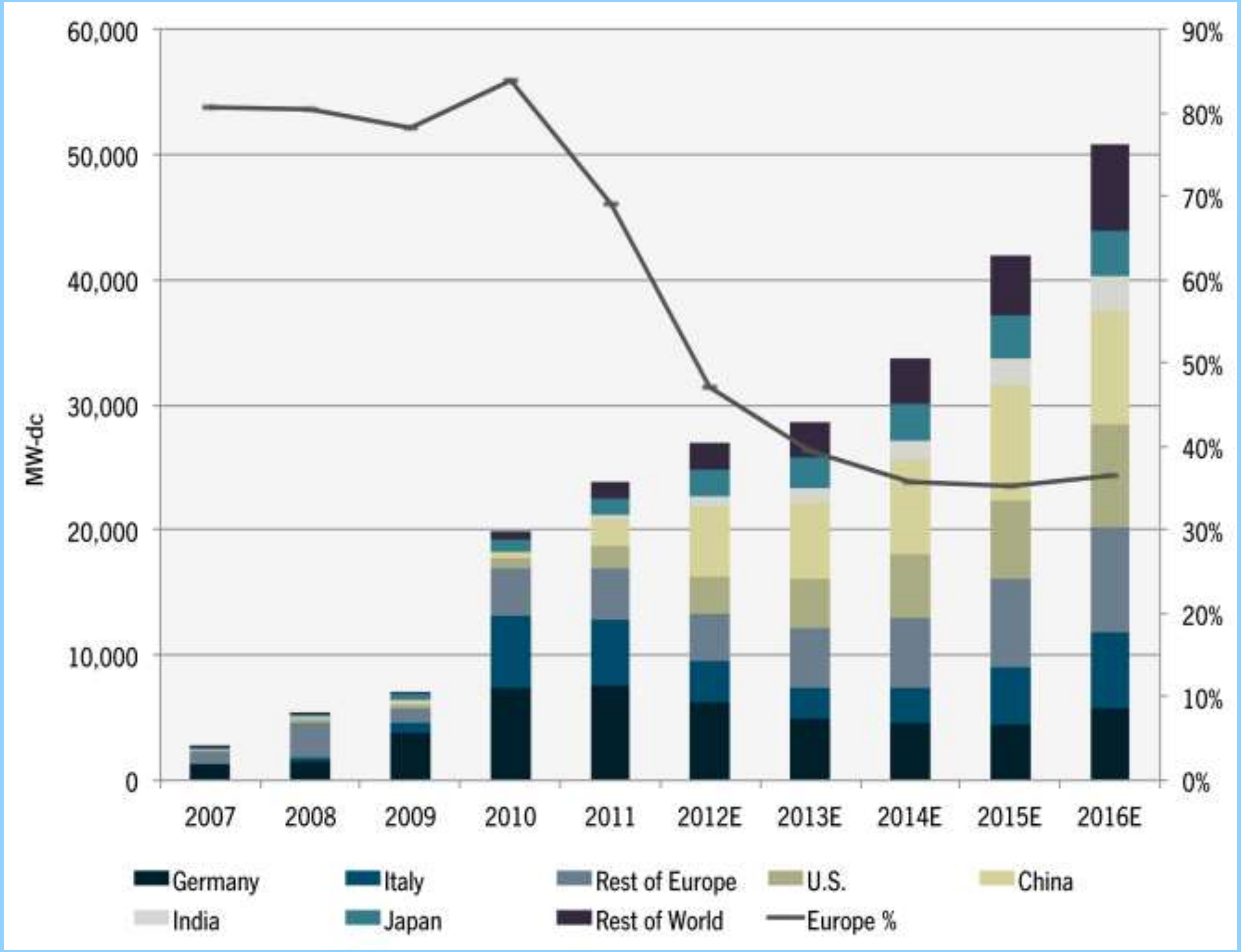


Cell group	Cell type	E_{ff} of cell [%]	E_{ff} of module [%]	Module producer
Crystalline Si	**Mono-crystalline (Cz-Si)**	24,7	22,7	SunPower – USA [3]
	Poly-crystalline (mc-Si)	20,3	18,6	Mitsubishi – Japan [4]
	Micro-crystalline (µc-Si)	11,7	10,9	Sanyo - Japan [1]
	Ribbon (R-Si)	-	13,4	Evergreen - USA [5]
	HIT	21,8	17,3	Sanyo – Japan [2]
High-performance	**GaAs**	25,8	-	-
	InP	21,9	-	-
	$GaInP_2$/GaAs	39,3	-	-
Thin-layer	**CdTe**	16,5	10,1	First Solar – USA [2]
	CIGS	19,5	12,2	Solibro - Germany [1]
	Amorphous Si (a-Si)	10,1	7,5	NES - China [6]
Organic	**Polymer**	5,1	1,8	Konarka - USA [6]
Photochemical	**Dye – Grätzel**	11,4	11,1	Sharp - Japan [3]

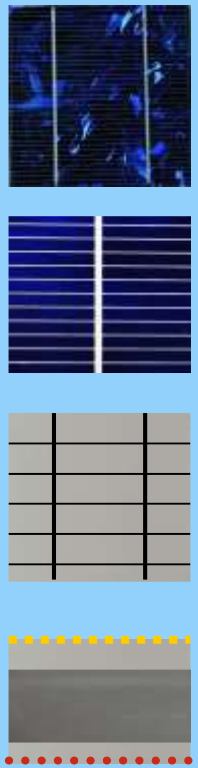
Proportional share of a given solar cell type in the total solar cell production of global photovoltaics in 2008



Annual Global PV Installations, 2007-2016E

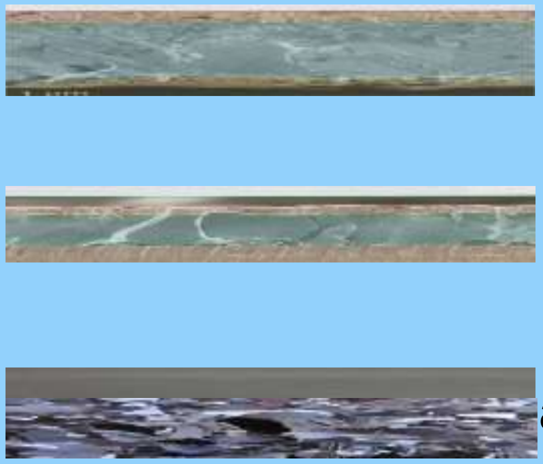


World manufakturing progress



PV „classical”modules

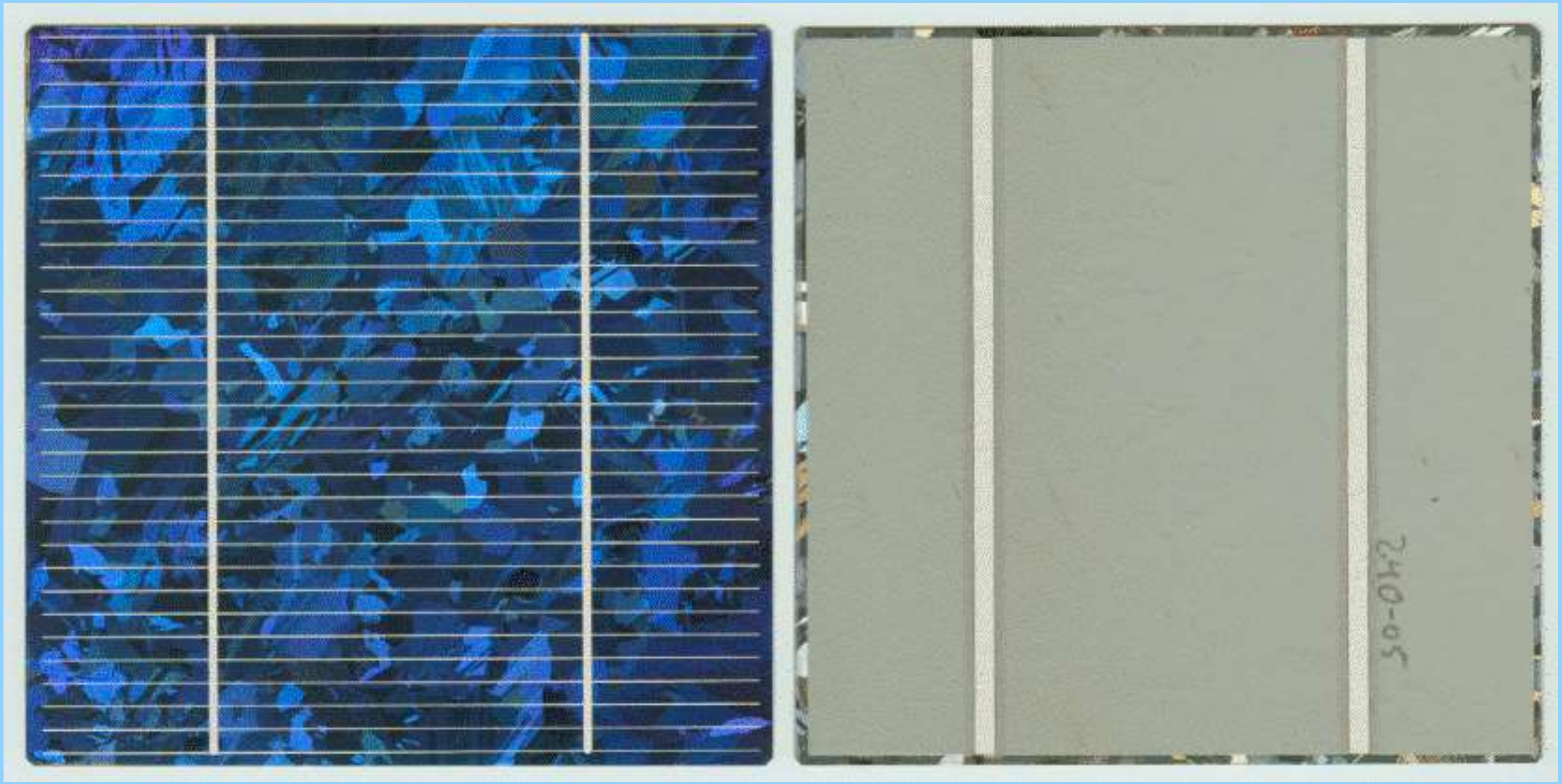
mc-Si	17 %
Cz-Si	19 %
R-Si	13 %
HIT	18 %



Thin film PV modules

CdTe	12 %
CIGS	15 %
a-Si/µc-Si	11 %

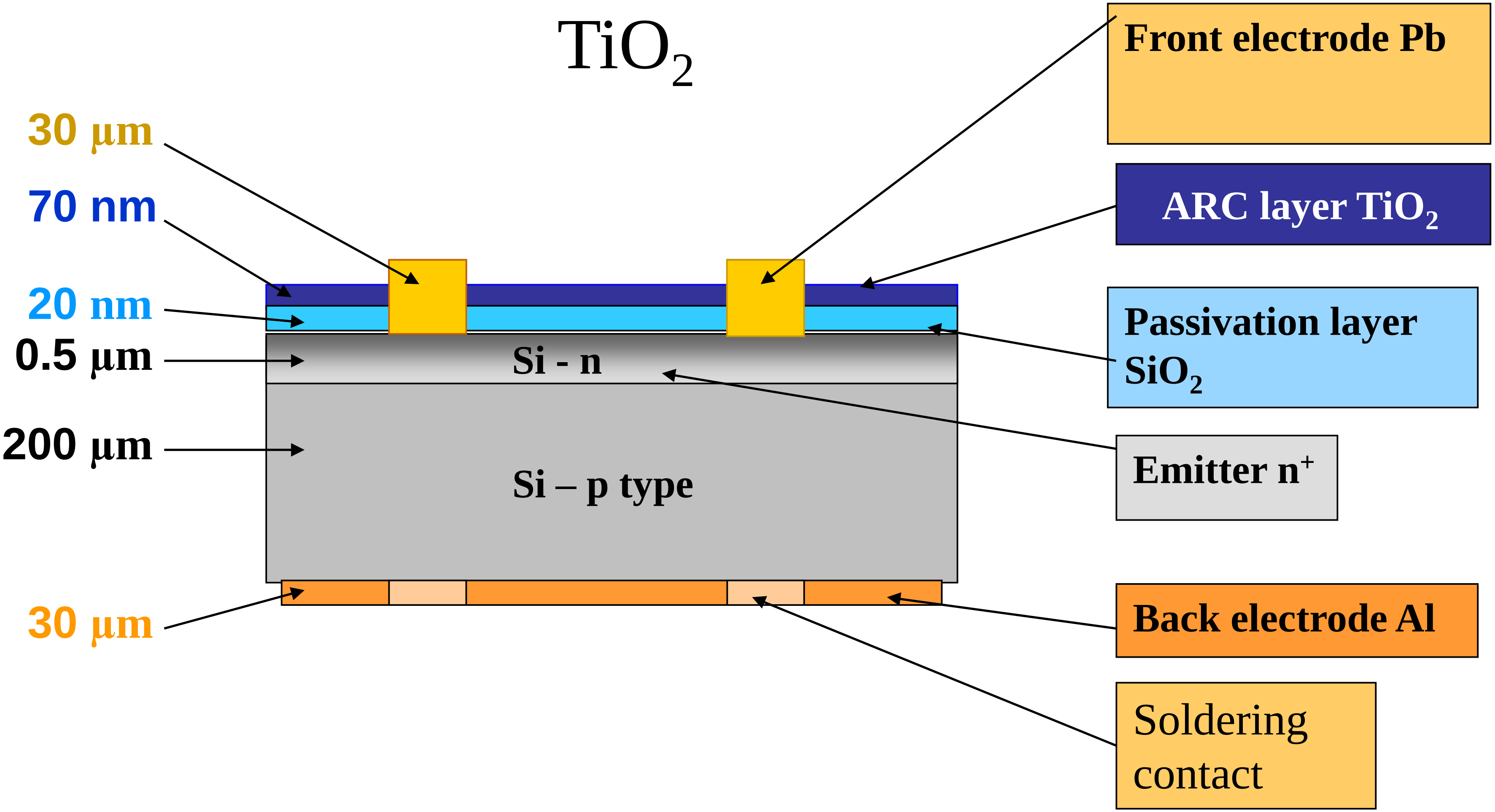
Crystalline Silicon Solar Cell on Multicrystalline Silicon



Front

Back

Scheme of solar cell section after metallization with TiO_2 as ARC layer



TiO_2

30 µm

70 nm

20 nm

0.5 µm

200 µm

30 µm

Si - n

Si – p type

Front electrode Pb

ARC layer TiO_2

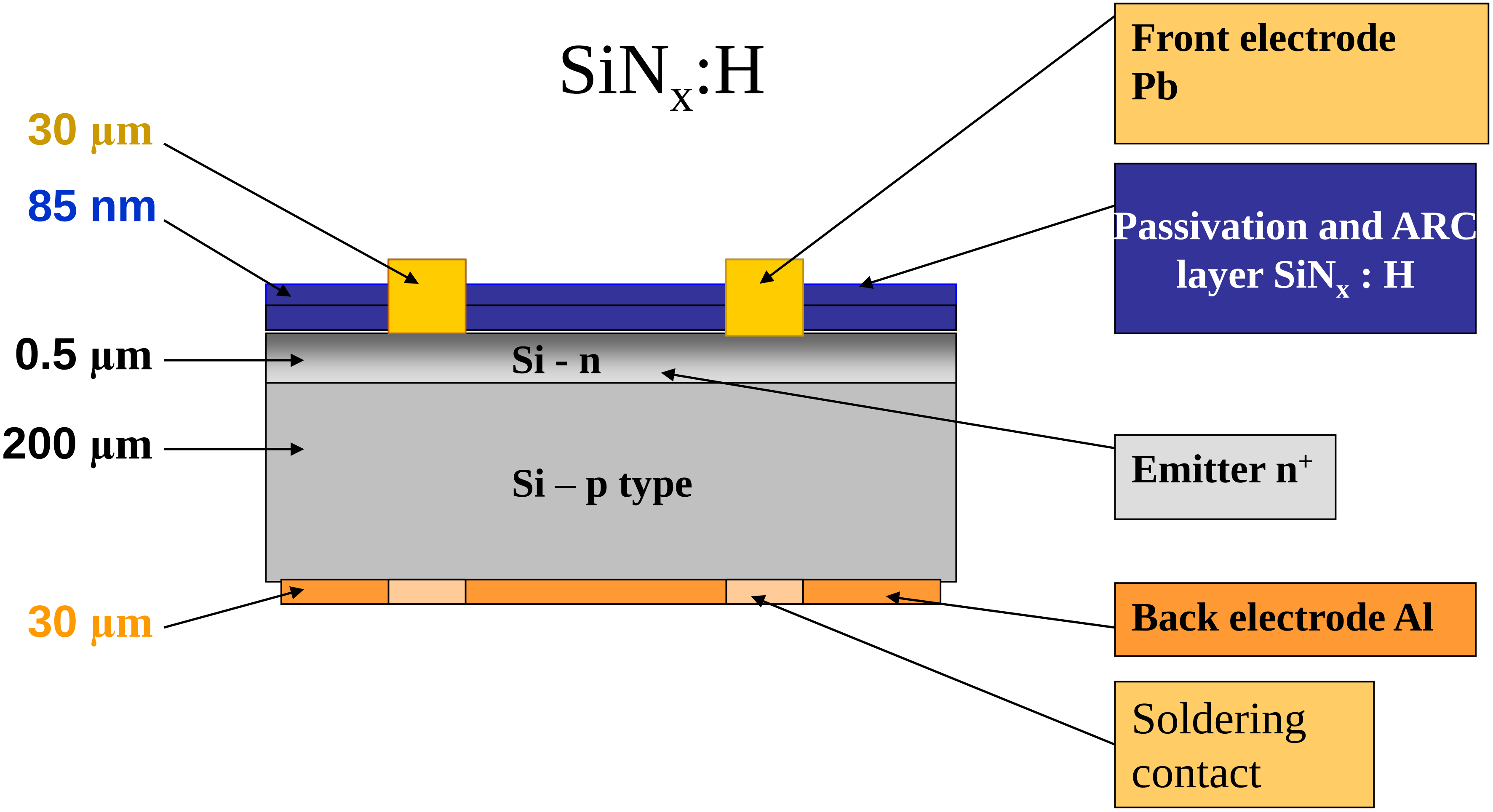
Passivation layer SiO_2

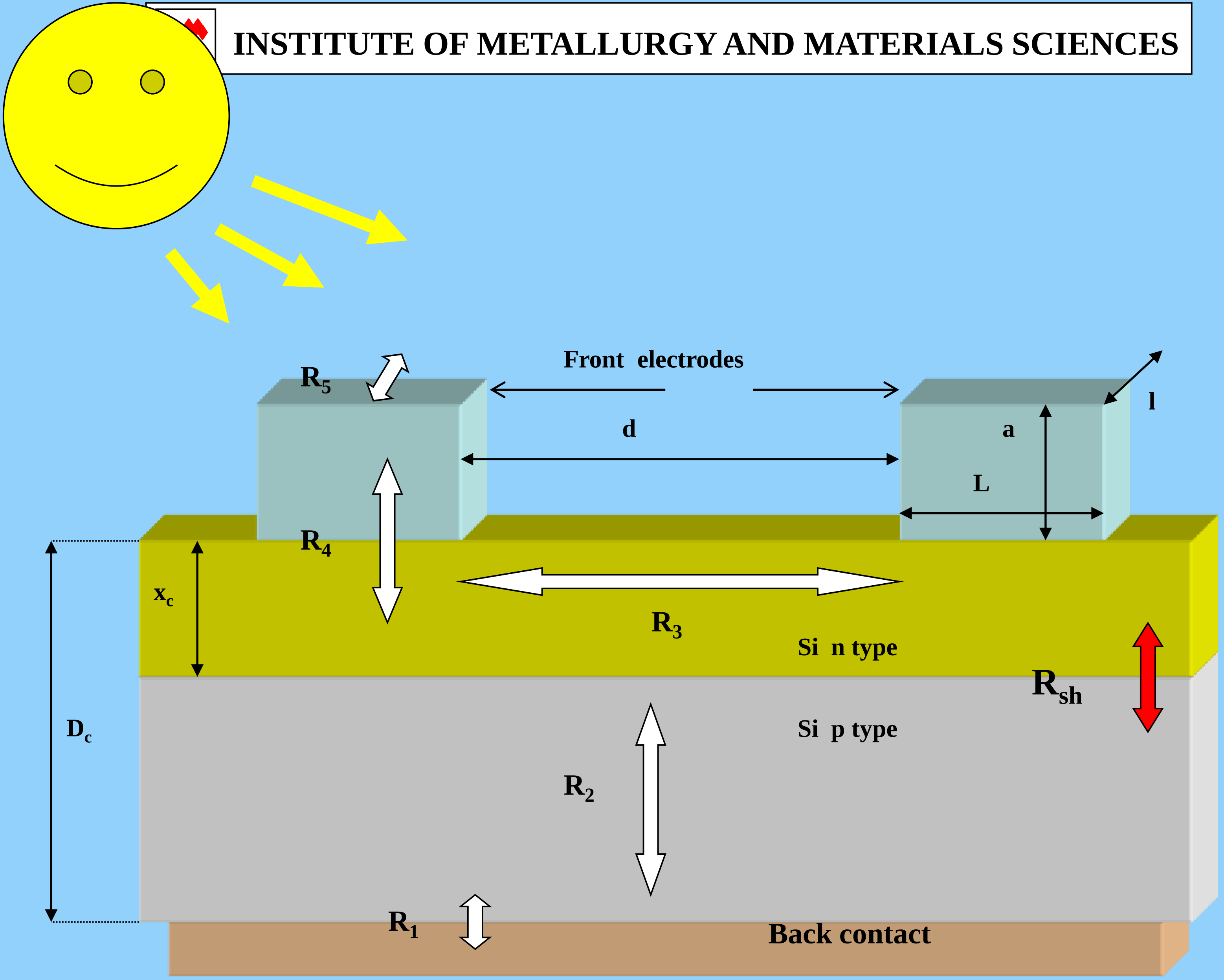
Emitter n^+

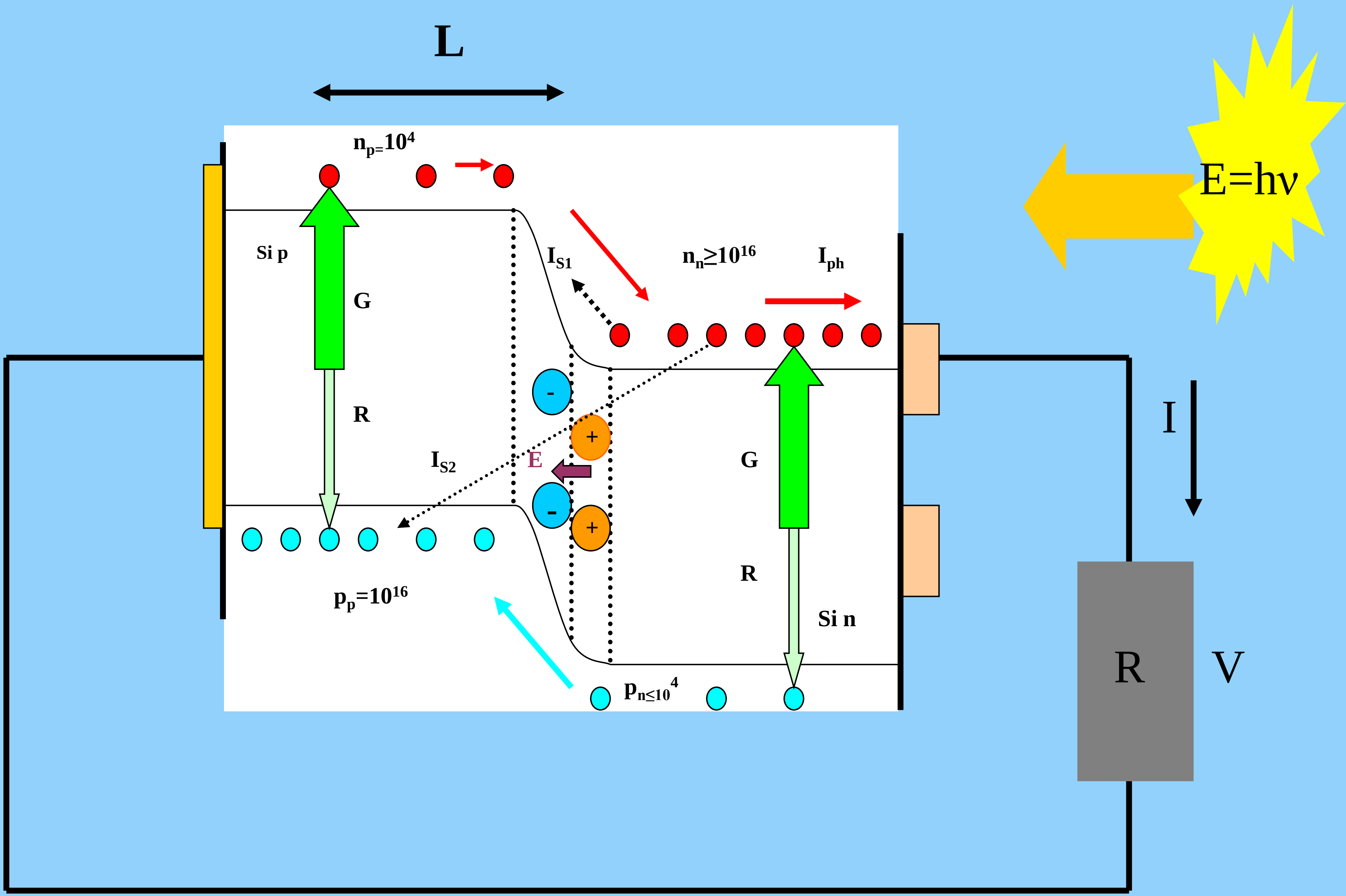
Back electrode Al

Soldering contact

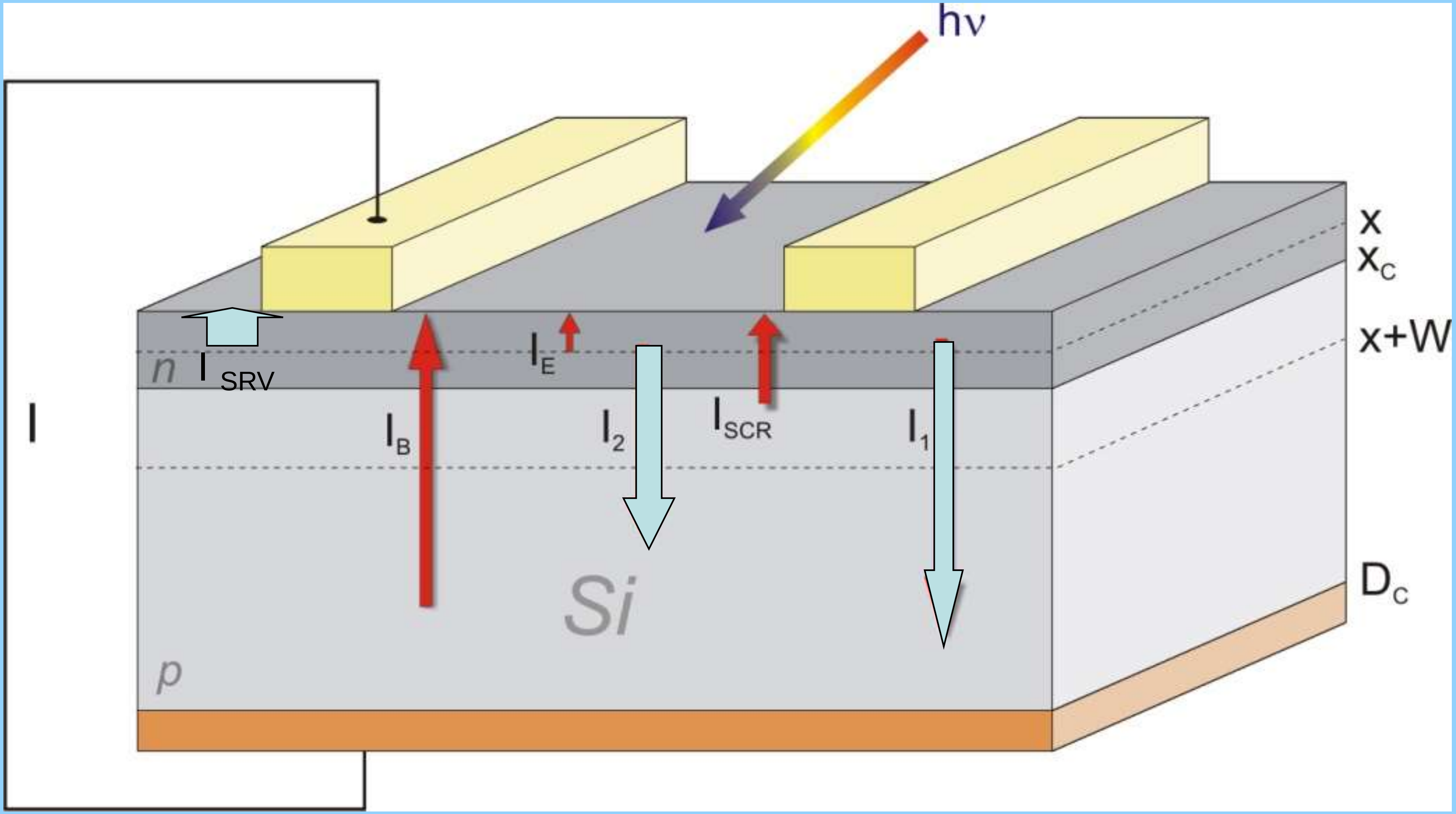
Scheme of solar cell section after metallization with SiN$_x$:H as ARC layer



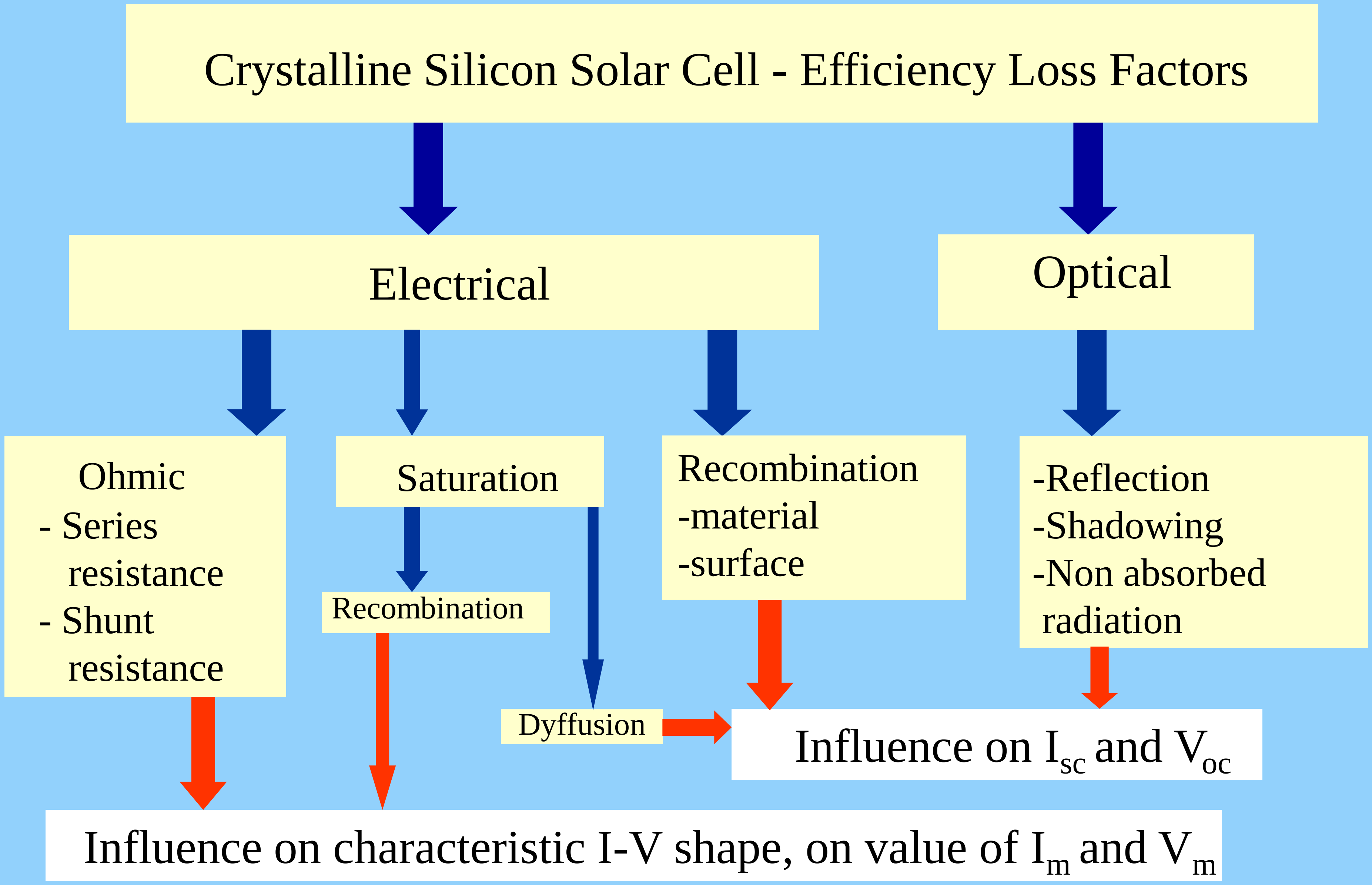

Front electrodes
R_5
d
a
l
L
R_4
x_c
R_3
Si n type
R_{sh}
D_c
Si p type
R_2
R_1
Back contact


L
$n_{p=}10^4$
Si p
G
R
I_{S1}
$n_n \geq 10^{16}$
I_{ph}
I_{S2}
E
-
+
-
+
G
R
Si n
$p_p=10^{16}$
$p_{n\leq 10}{}^4$
E=hν
I
R
V

Scheme of electron current component of a solar cell.
W is the width of the space charge area and x_c is the depth of the p-n junction’s position.



Crystalline Silicon Solar Cell - Efficiency Loss Factors



Electrical

Optical

Ohmic
- Series resistance
- Shunt resistance

Saturation

Recombination

Dyffusion

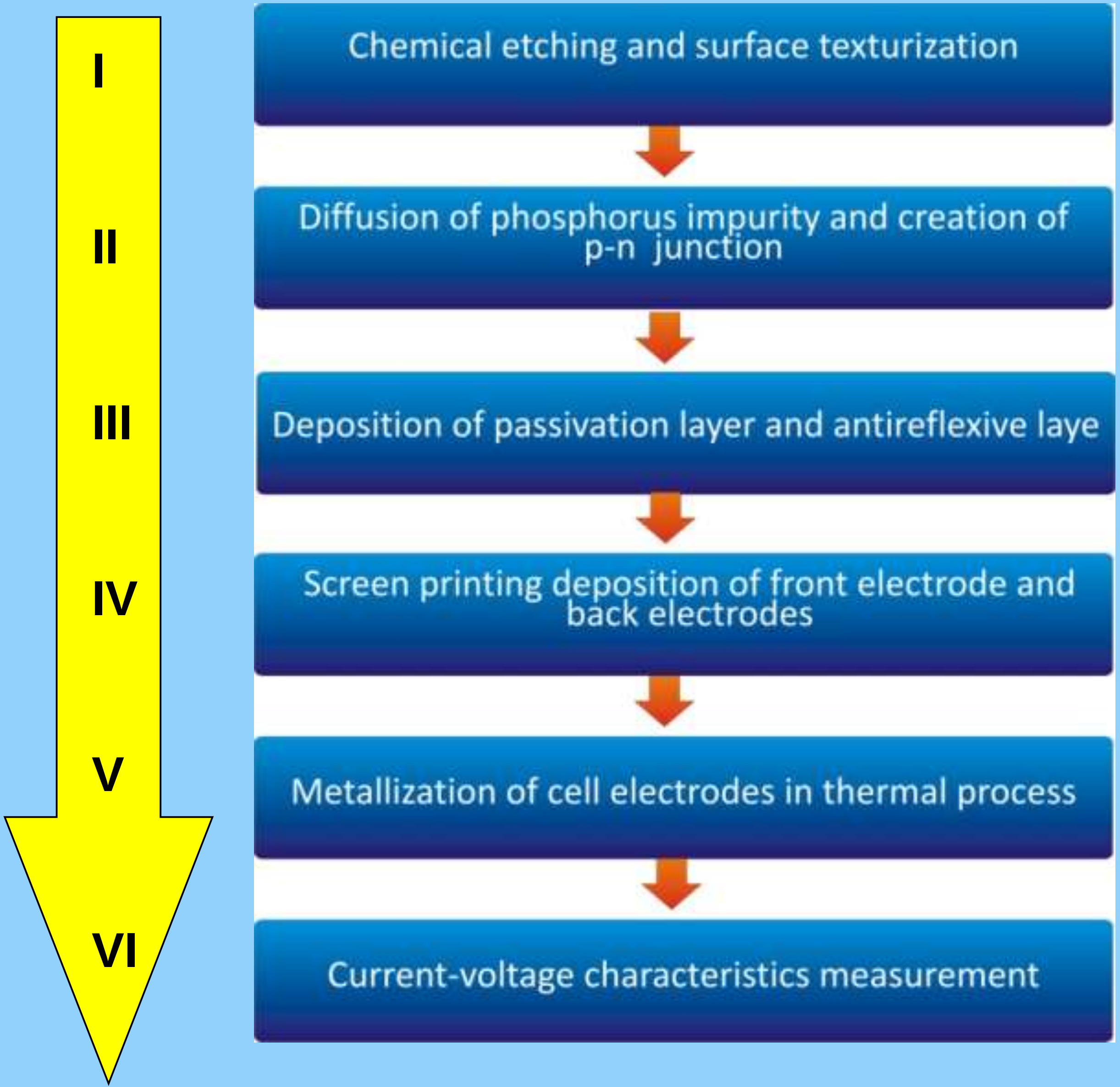
Recombination
-material
-surface

-Reflection
-Shadowing
-Non absorbed radiation

Influence on I_{sc} and V_{oc}

Influence on characteristic I-V shape, on value of I_m and V_m

Scheme of the technological process of silicon solar cell production



I Chemical etching and surface texturization

II Diffusion of phosphorus impurity and creation of p-n junction

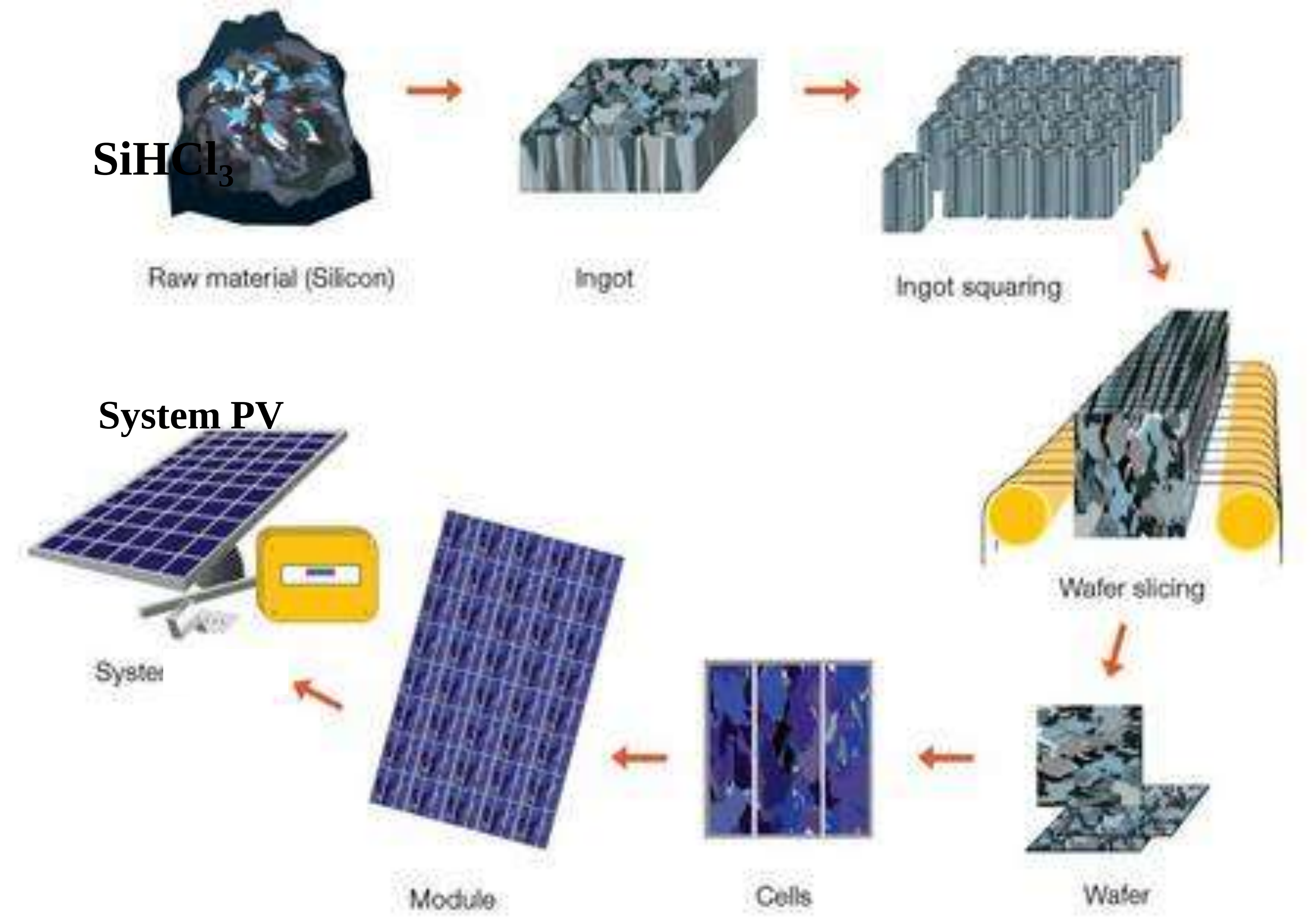
III Deposition of passivation layer and antireflexive laye

IV Screen printing deposition of front electrode and back electrodes

V Metallization of cell electrodes in thermal process

VI Current-voltage characteristics measurement

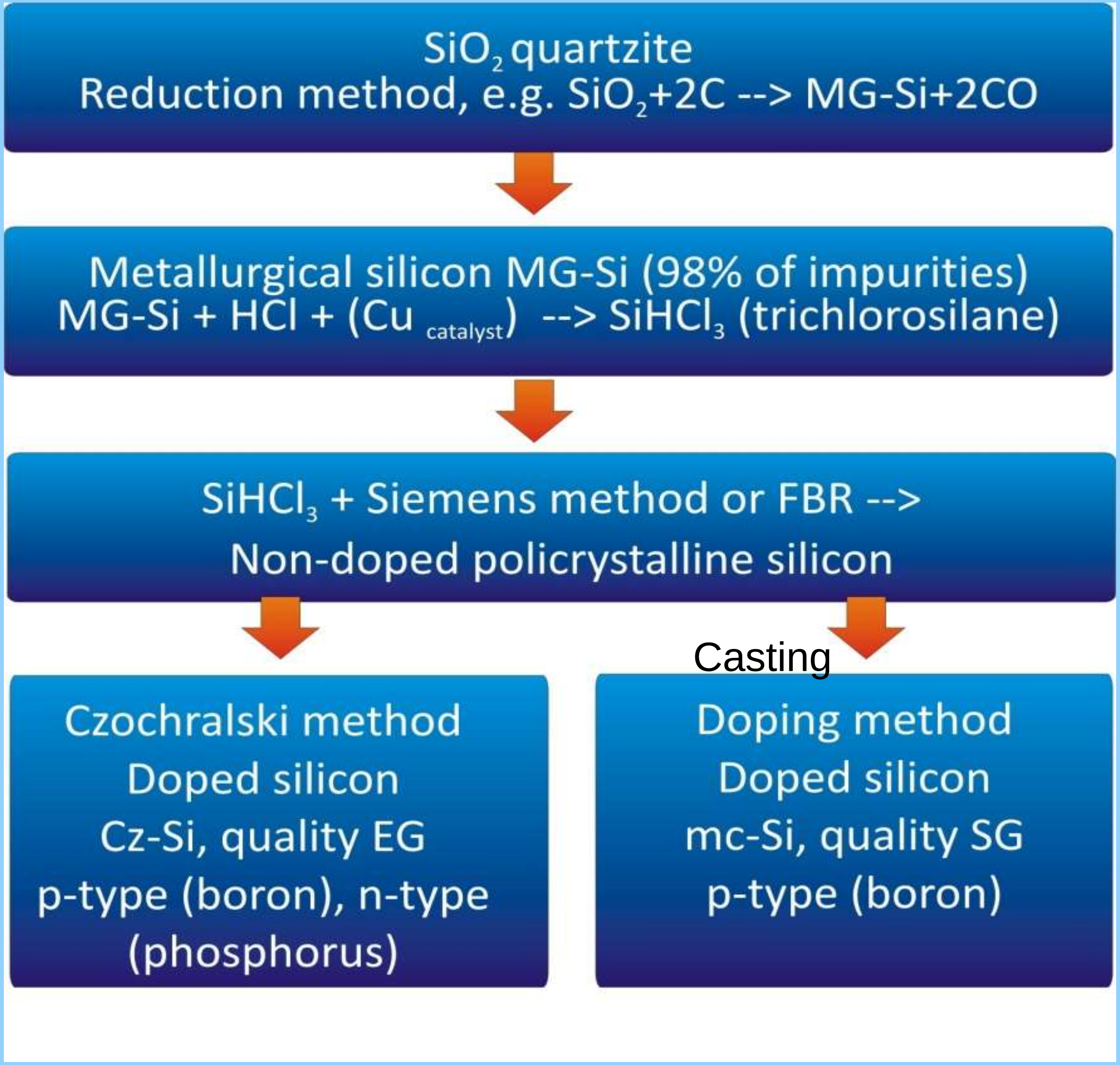
The way from SiO_2 to PV system



Where from the crystalline silicon came ?

The PV sector involves the production of polycrystalline silicon (mc-Si) type p by means of casting, which is often called the multicrystalline silicon due to the big sections of its grains. Crystalline silicon used in photovoltaics is referred to as the SG (*Solar Grade*) silicon and its quality is lower than that which is used in electronics and which is designated as the EG (*Electronic Grade*) silicon, in which an exemplary value of carbon equals 0,1 ppm (5×10^{15} atoms/cm^3) and the oxygen content is 0,01 ppm.

Scheme of the production process of crystalline silicon for the IC and PV sectors



SiO_2 quartzite
Reduction method, e.g. $SiO_2 + 2C \rightarrow$ MG-Si+2CO

Metallurgical silicon MG-Si (98% of impurities)
MG-Si + HCl + ($Cu_{catalyst}$) --> $SiHCl_3$ (trichlorosilane)

$SiHCl_3$ + Siemens method or FBR -->
Non-doped policrystalline silicon

Czochralski method
Doped silicon
Cz-Si, quality EG
p-type (boron), n-type (phosphorus)

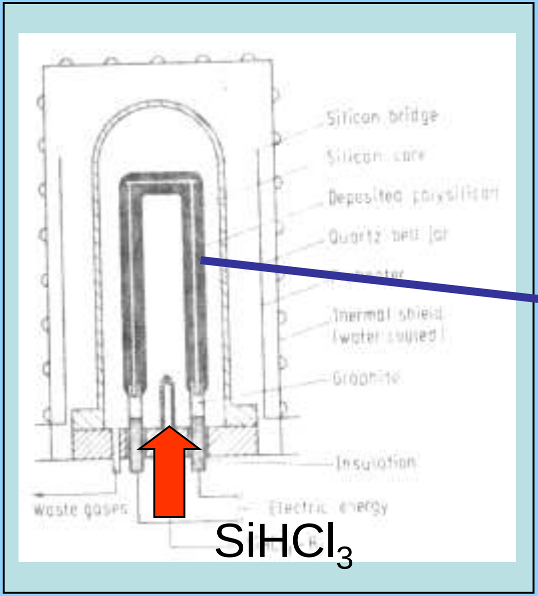
Casting

Doping method
Doped silicon
mc-Si, quality SG
p-type (boron)

Three of the biggest producers of non-doped polycrystalline silicon, which are Hemlock (USA), Wacker (Germany) i Tokuyama (Japan), apply the Siemens method, in which polycrystalline silicon, 20 cm in diameter, is created in a trichlorosilane reactor, on a crystalline silicon bar, 10 mm in diameter, heated up to 1100 ^{o}C. This process takes a few days and requires the provision of 200 kWh electric energy in order to obtain 1 kg of silicon. In an alternative method, FBR *(Fluidised Bad Reactor), the polycrystals of silicon are created in the form of granulate, in a continuous process* with $SiHCl_3$ at the temperature of 1000 ^{o}C, or SiH_4 at the temperature of 700 ^{o}C. The method which allows for a further purification of the mc-Si silicon and the obtaining of mono-crystalline silicon is zone melting, in which the FZ (*Float Zone) silicon is* obtained. The basic method of the Si mono-crystal production for the electronic industry is the Czochralski method.

The SIEMENS method

Scheme of the Siemens method



J. L. Vossen, W. Kern,
Thin film process,
Academic Press,
New York, 1978

Kreutzmann,"Robin Hoods of PV",
Photon International, 9, 2006, str.58.

Renewable Energy World, 9, 2006, str.4.

Where from the silicon come ?

Virgin Feedstock – Material shown manufactured by Hemlock, USA

Poly with Popcorn Surface

Poly Tear Drops

Poly Seed Rods

Tops & Tails

Other Material

- Off spec silicon rods
- Crucible bottoms
- Wafer scrap from semiconductor industry

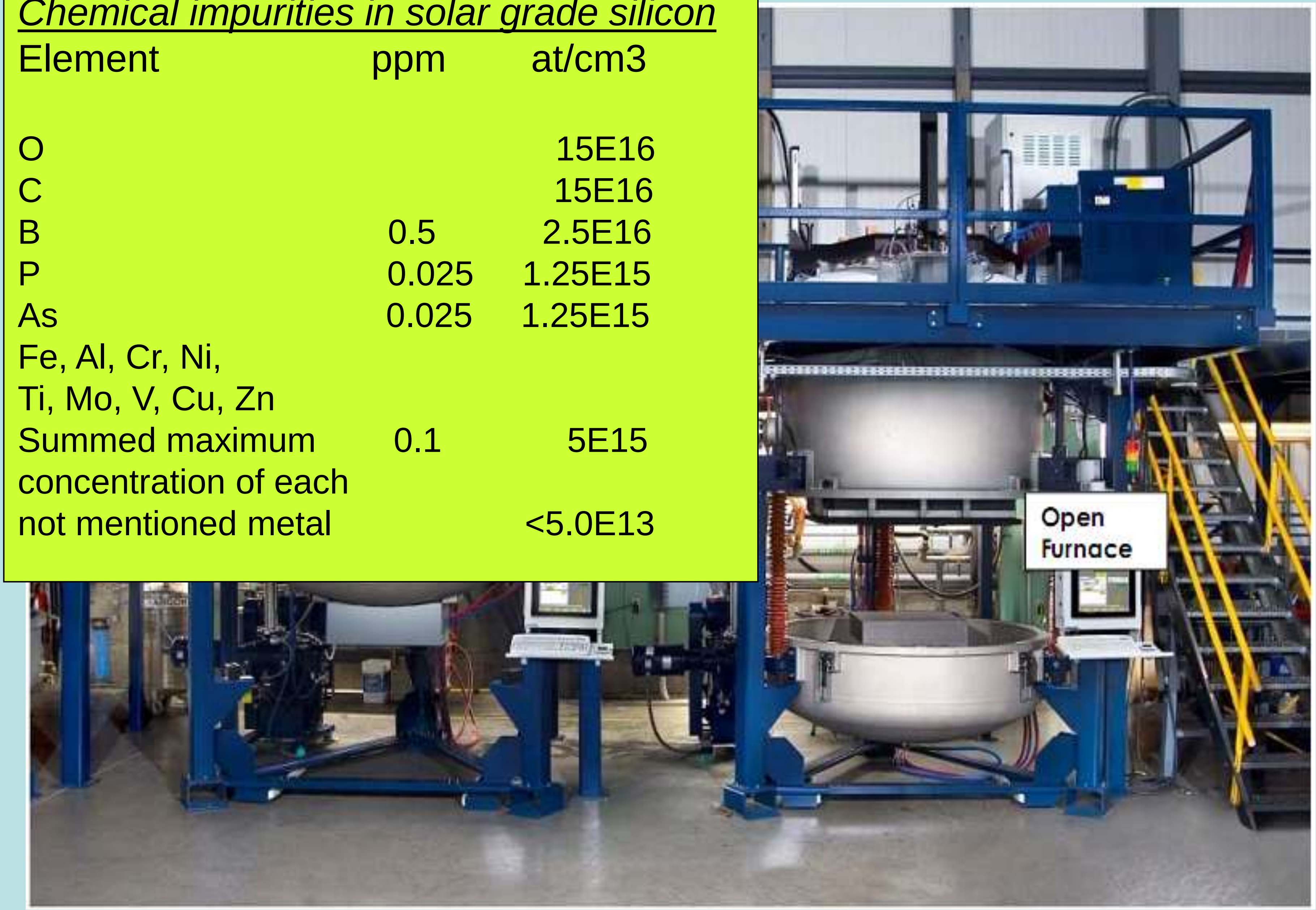
Pot Scrap

Casting in crucible


Closed Furnace
Open Furnace

Chemical impurities in solar grade silicon

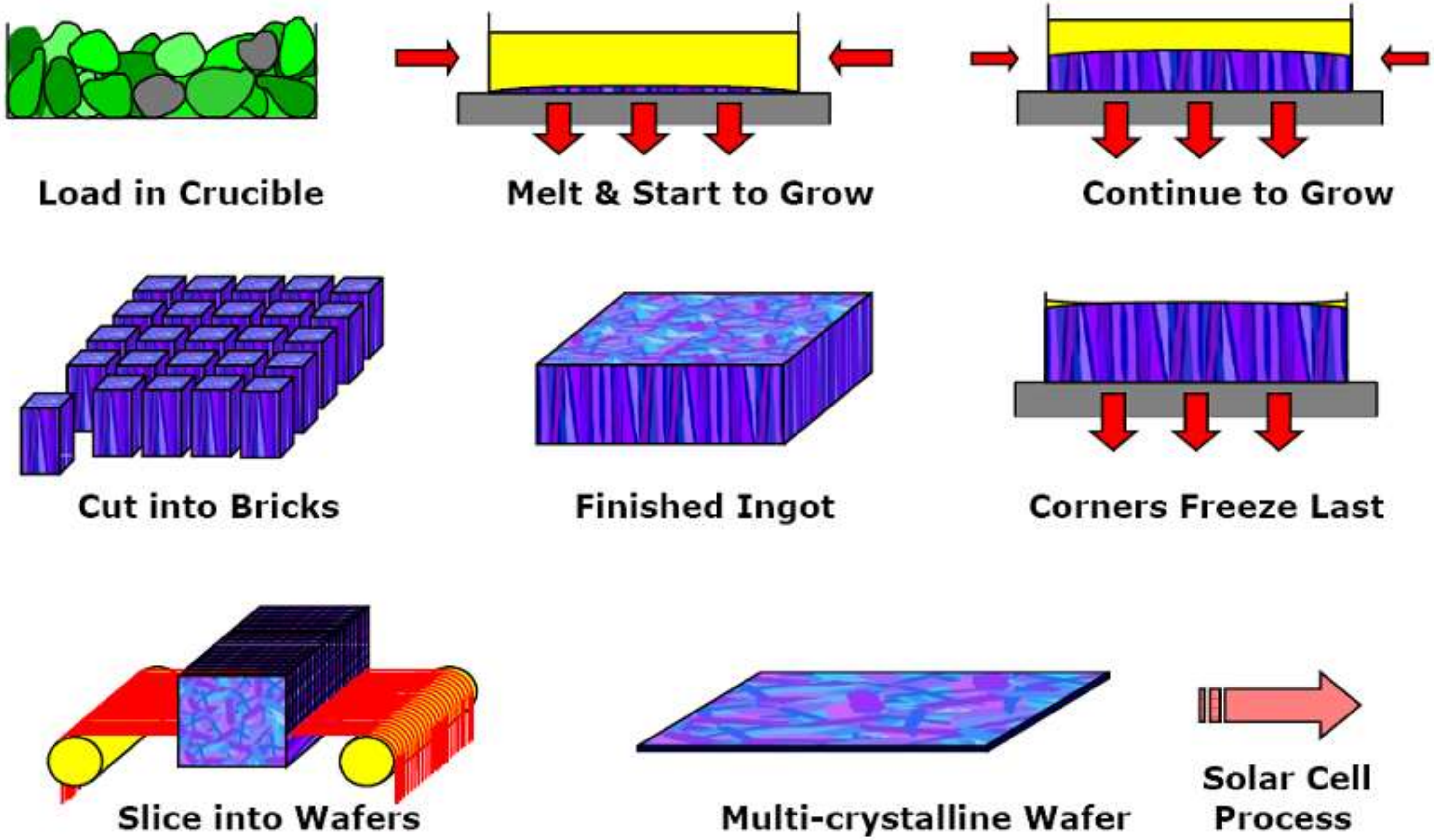
Element	ppm	at/cm3
O		15E16
C		15E16
B	0.5	2.5E16
P	0.025	1.25E15
As	0.025	1.25E15
Fe, Al, Cr, Ni, Ti, Mo, V, Cu, Zn Summed maximum	0.1	5E15
concentration of each not mentioned metal		<5.0E13



Si quasi-mono crystalline

Blok
Q-Si

Cz-Si



Load in Crucible

Melt & Start to Grow

Continue to Grow

Corners Freeze Last

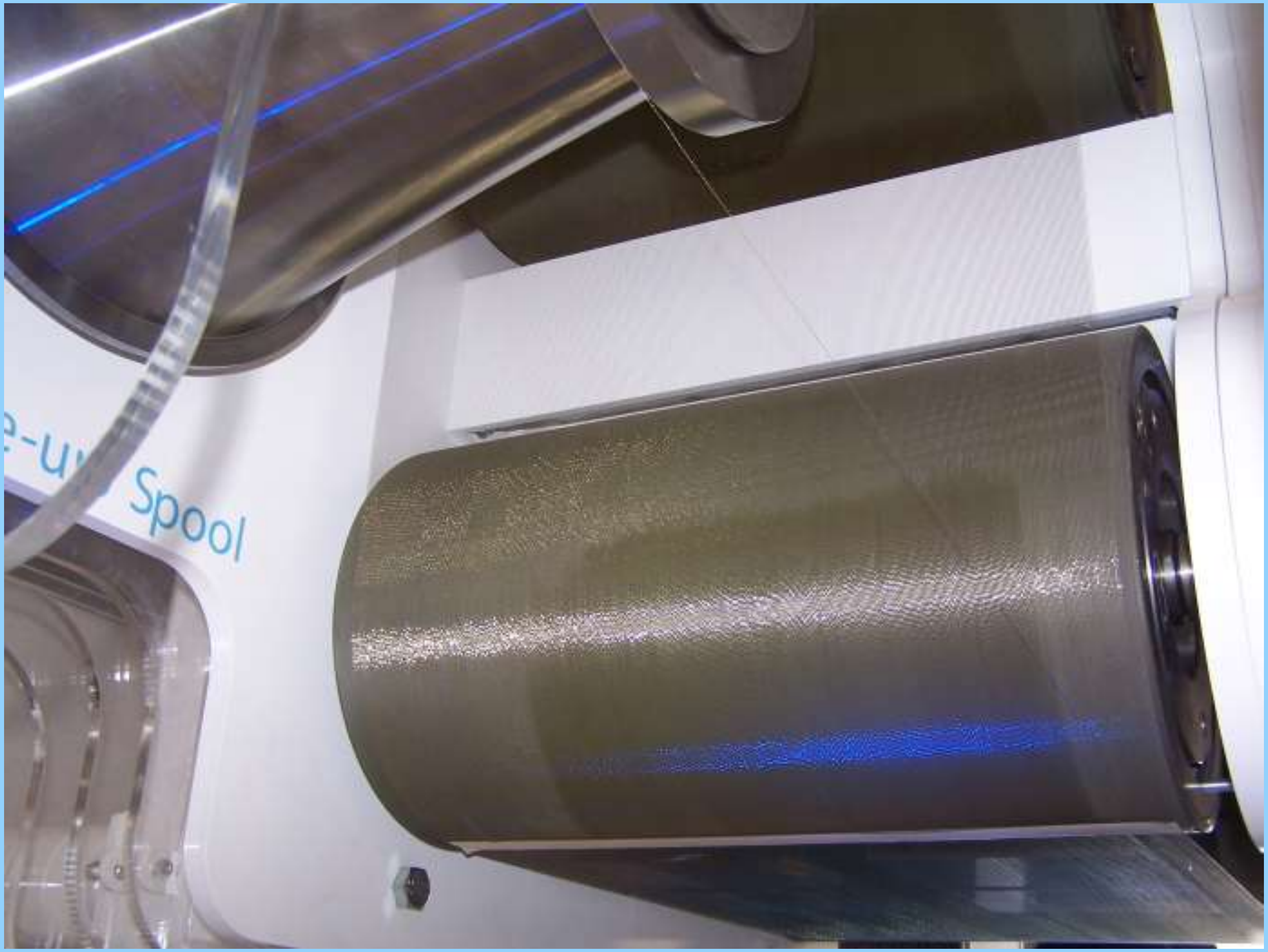
Finished Ingot

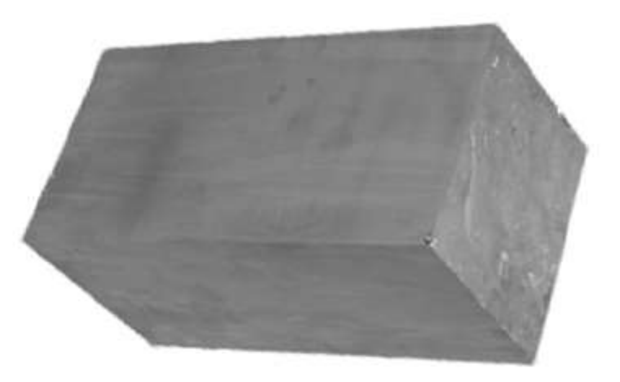
Cut into Bricks

Slice into Wafers

Multi-crystalline Wafer

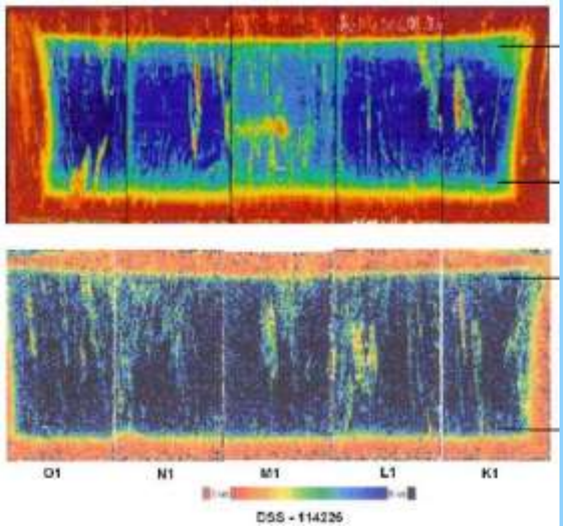
Solar Cell Process

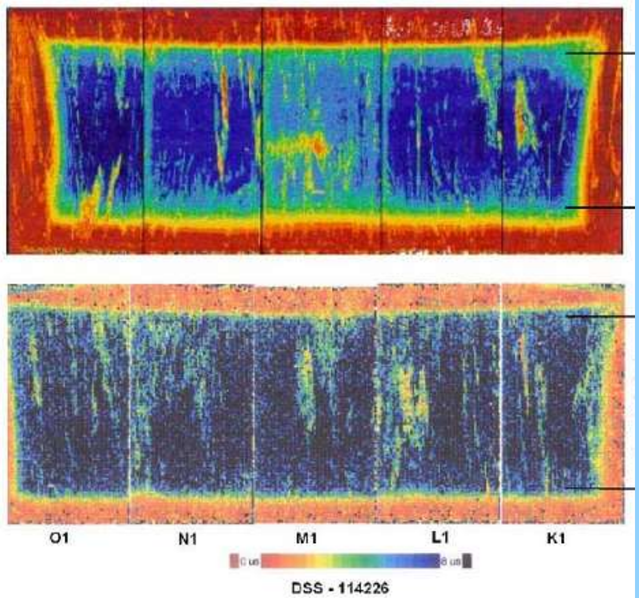

e-u Spool

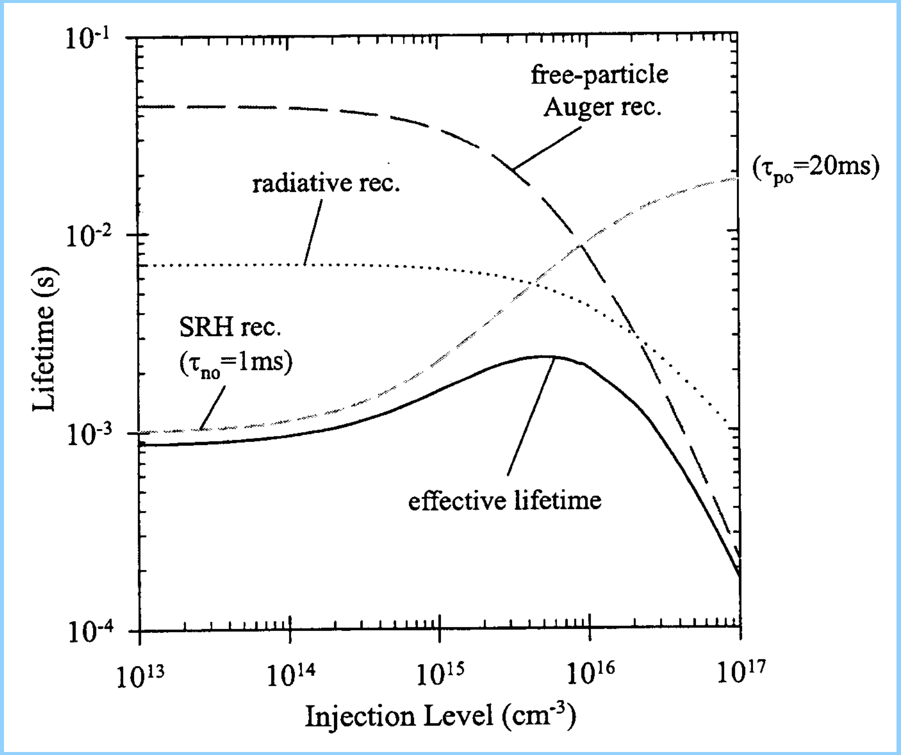


The catting process
by saw wire

The influence
of cutting process
on effective
lifetime







Effective lifetime

$$1/\tau_{(bulk)or(surface)or(emitter)} = 1/\tau_{rad} + 1/\tau_{Auger} + 1/\tau_{SRH}$$

$$1/\tau_{effective} = 1/\tau_{bulk} + 1/\tau_{Fsurface} + 1/\tau_{Bsurface} + 1/\tau_{emitter}$$

Tha basic correlation between τ and L

$$1/\tau_{(bulk)or(surface)or(emitter)} = 1/\tau_{rad} + 1/\tau_{Auger} + 1/\tau_{SRH}$$

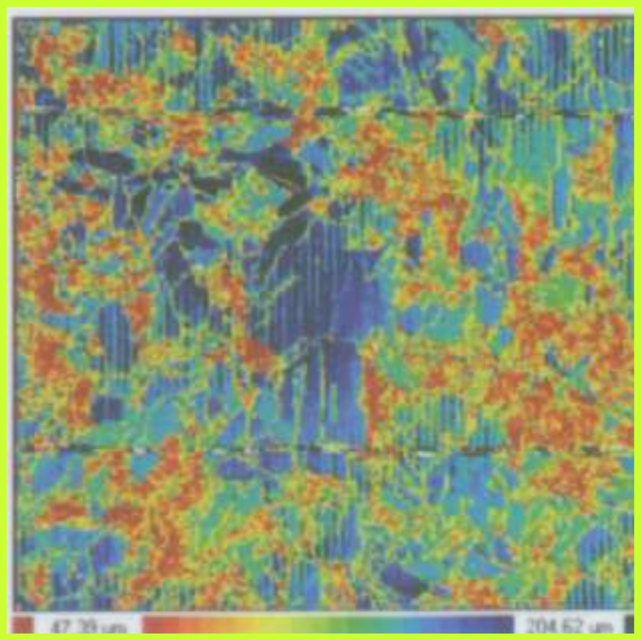
L is the diffusion length of the charge carriers, the electrons and the holes, connected with their lifetime τ by the following relation:

$$\mathrm{L} = \sqrt{\mathrm{D}\tau}$$

where: $D = \mu kT/q$ is the carrier diffusion coefficient of mobility μ.

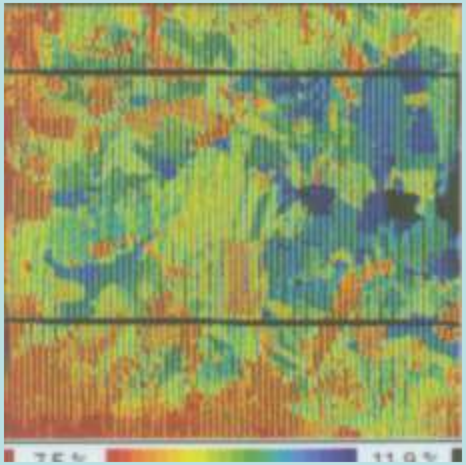
LBIC

Seperation – 100 µm

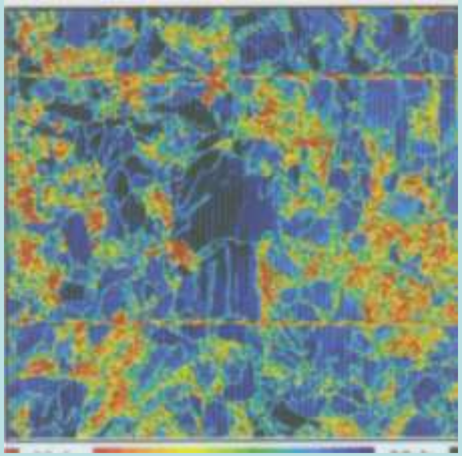


Diffusion length

Laser = 980 nm

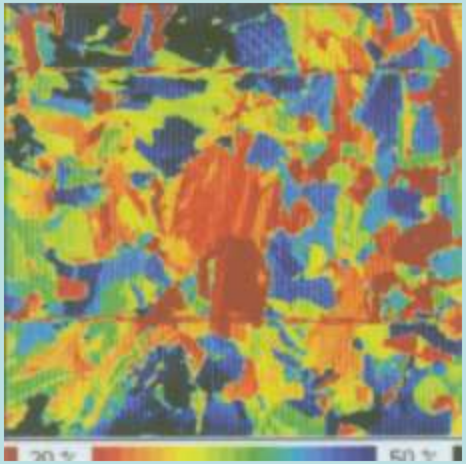


R_{eff}

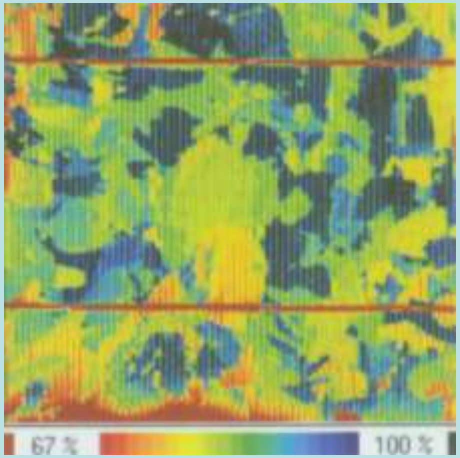


IQE

Laser = 405 nm

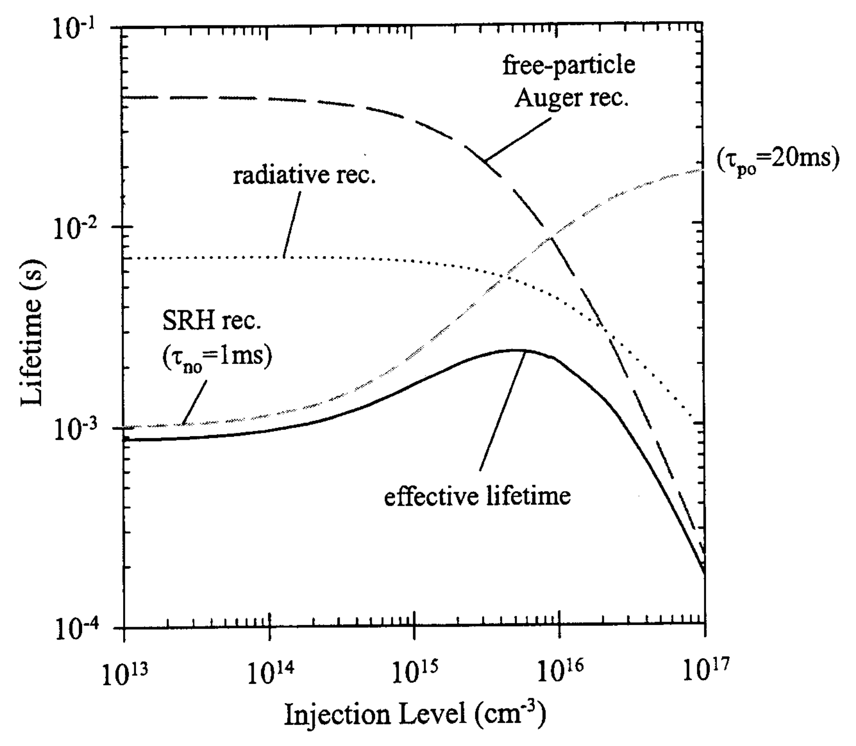


R_{eff}

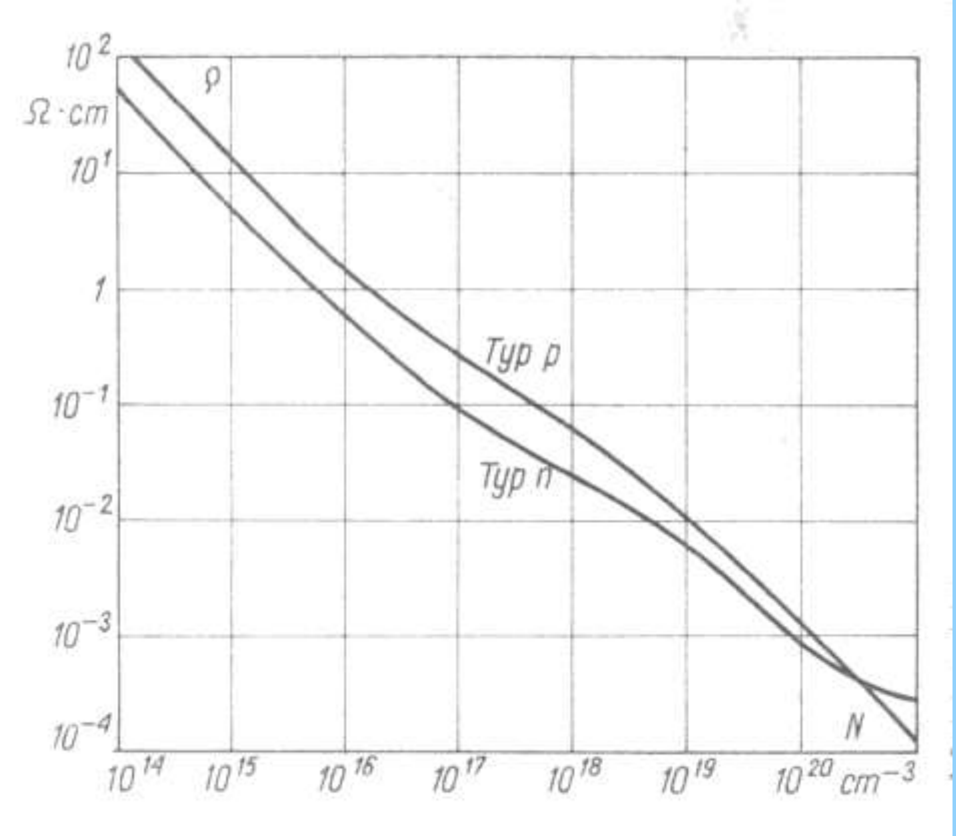


IQE

Lifetime of the charge carriers



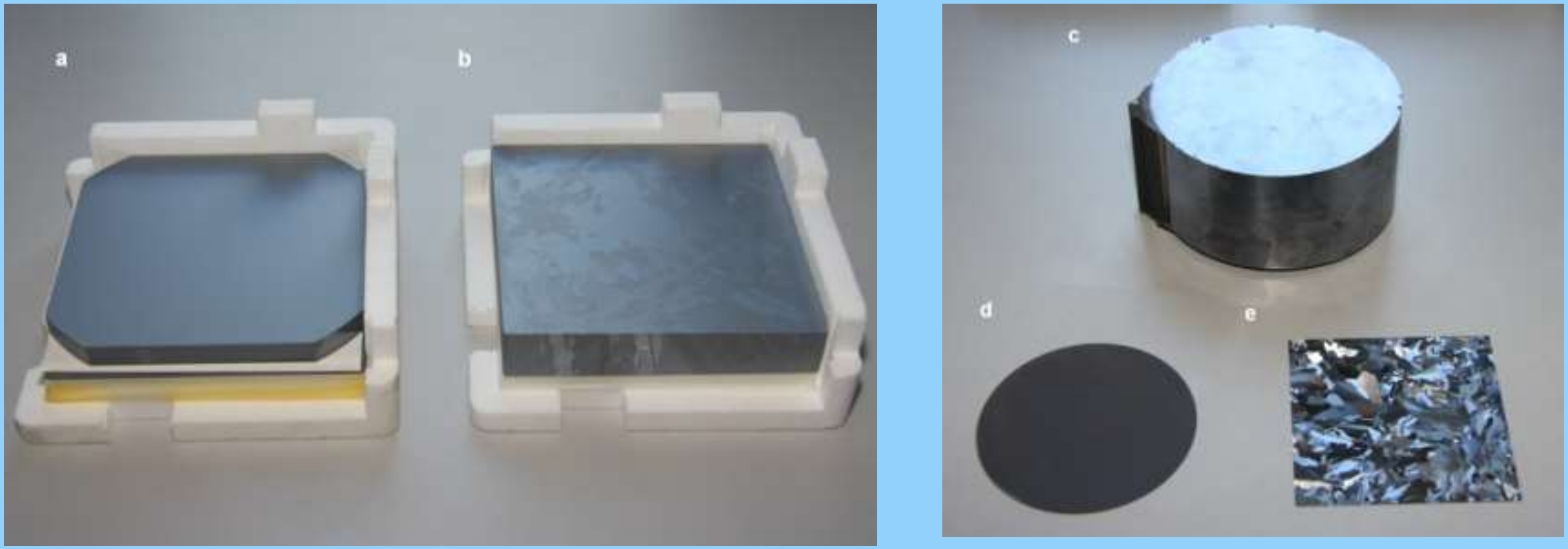
The dependence of Si resistivity
on dopent concentration at 300 ºK



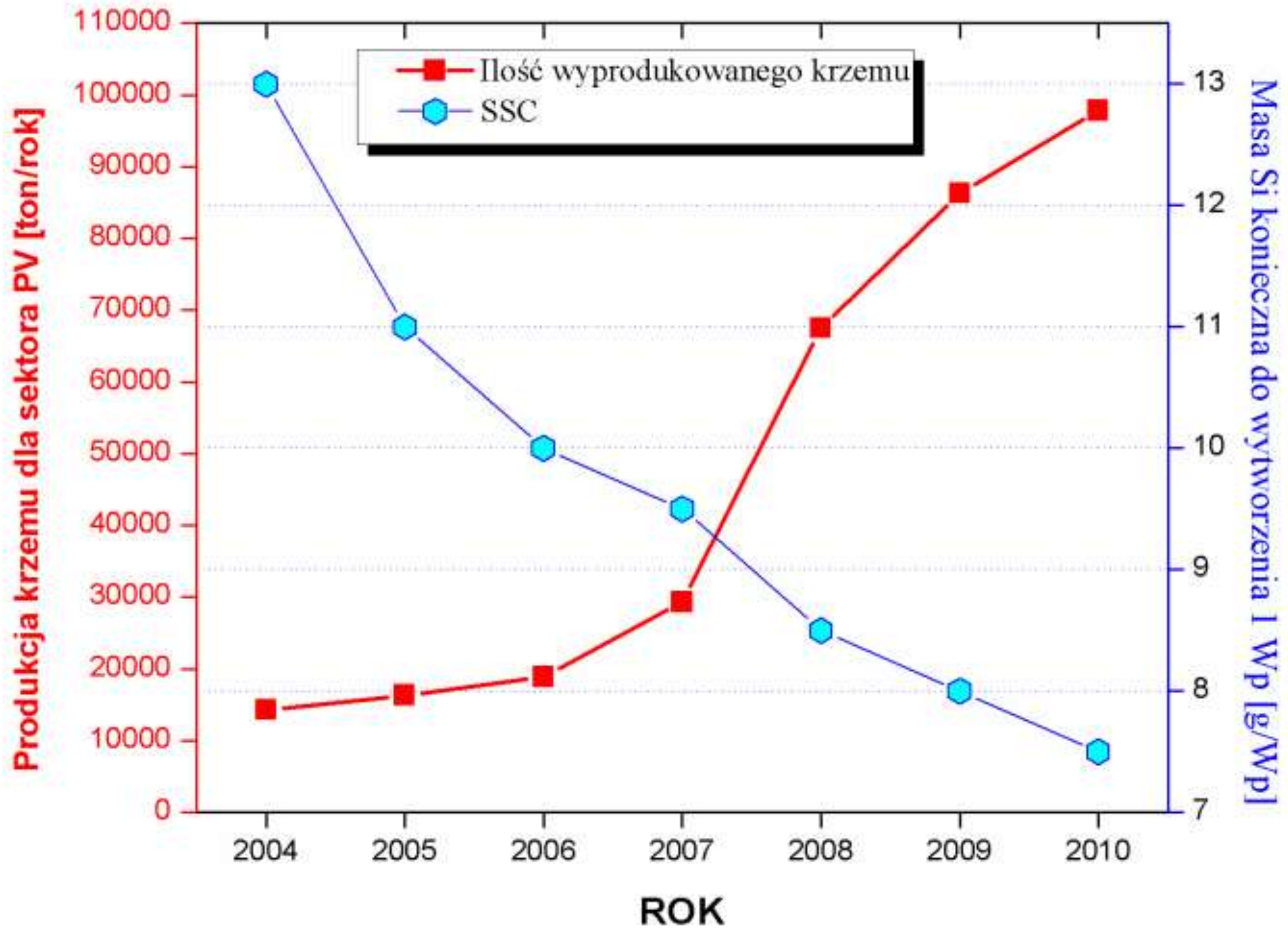
The resistance of a wire
L - longest A - diameter
$R = \rho \cdot L / A$
$\Omega = \Omega\text{cm} \cdot \text{cm} / \text{cm}^2$

Procesy technologiczne w elektronice
półprzewodnikowej, WNT, Warszawa 1973, str. 246

I Chemical etching and surface texturization



Provided by the producer, original pack of 125 items of six-inch mono-crystalline silicon wafers Cz-Si (a) and poly-crystalline silicon plates mc-Si (b), 200 μm thick, used in the solar cell production. Fragment of a silicon Cz-Si roller made with the Czochralski process (c) and the cut-out plate used in the IC *(Integrated Circuit) sector* (d), next to a four-inch single mc-Si silicon plate, after the elimination of the defected layer, resulting from the block sawing (e).


Ilość wyprodukowanego krzemu
SSC
Produkcja krzemu dla sektora PV [ton/rok]
110000
100000
90000
80000
70000
60000
50000
40000
30000
20000
10000
0
Masa Si konieczna do wytworzenia 1 Wp [g/Wp]
13
12
11
10
9
8
7
2004
2005
2006
2007
2008
2009
2010
ROK

I Chemical etching and surface texturization

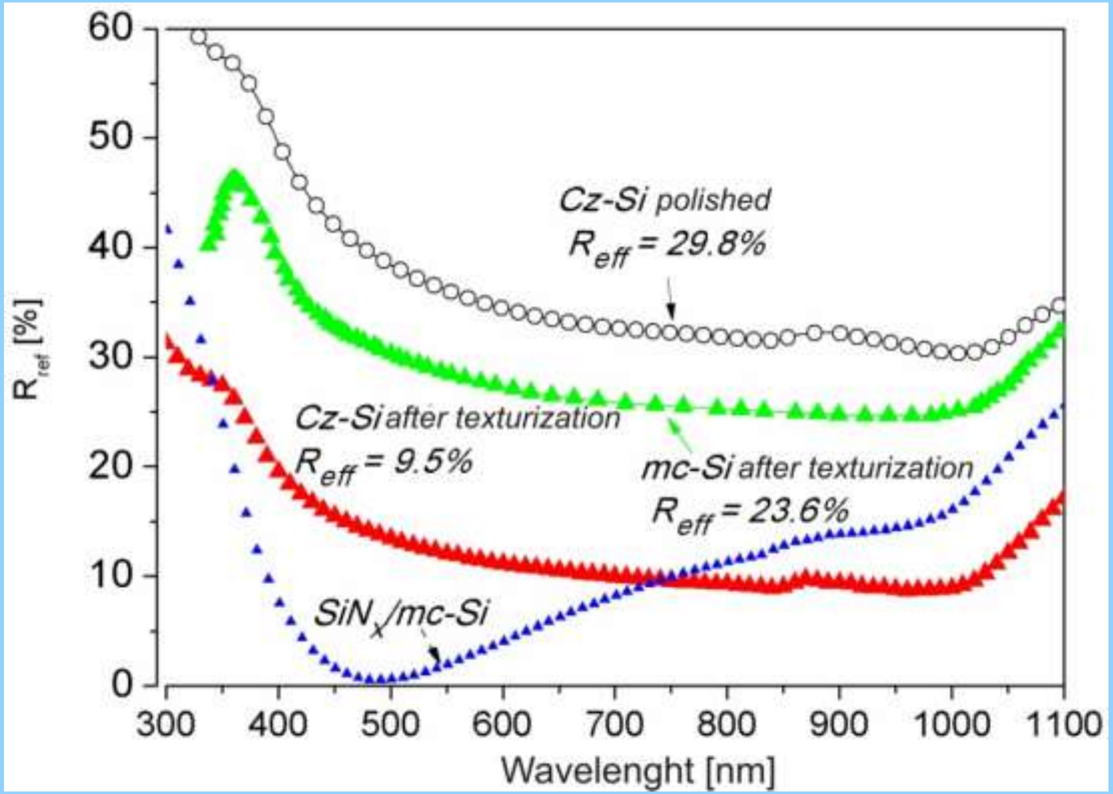
Chemically prepared silicon pates placed in teflon holders (left) and chemical etching process (right)

Si p type, resistivity 1 ohmcm, thickness ~ 200 μm, τ - 5 ÷ 25 μs

I Chemical etching and surface texturization

The mc-Si and Cz-Si silicon plates obtained from the producer have a defected surface, down to the depth of ~ 5 µm, formed as a result of diamond or wire saw cutting. The two-sided elimination of the defected layer is performed in the process of chemical etching in a KOH solution. In order to reduce the reflection coefficient Rref, the surface of the plate is covered with texture. In the case of Cz-Si, the surface texturization is performed in the chemical process at the temperature of 80 ^{o}C for the time of 30 min. In a KOH:IPA:H2O solution, the texturization of the mc-Si plates is conducted on the basis of the $HF:HNO_3:H_2O$ acid solutions. In the next stage, which aims at the elimination of organic and metallic impurities, as well as natural oxides, the Si plates are placed in baths of H_2SO_4, HCl and HF solutions, respectively. Between each stage, the plates are rinsed in deionized water of resistivity not lower than 5 MΩcm. The reagents used in these processes must be in the chemical purity class of ”analytically pure”. Because of the applied types of chemical solutions, the plates are placed in teflon holders.

I Chemical etching and surface texturization

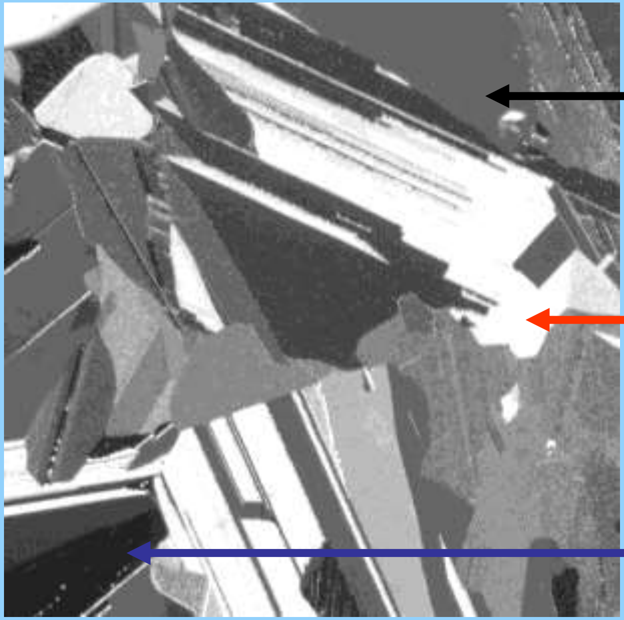


Dependence of the reflection coefficient on the wavelength for surface-polished silicon Cz-Si and mc-Si, after texturization and deposition of a silicon nitride ARC layer; measurements performed with a spectrophotometer Perkin-Elmer Lambda-19, at AGH, Krakow.

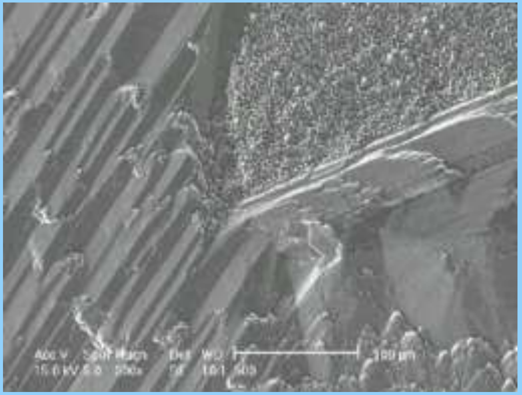
Looking for reflectivity reduction

Texturization

Mc-Si after etching in KOH solution



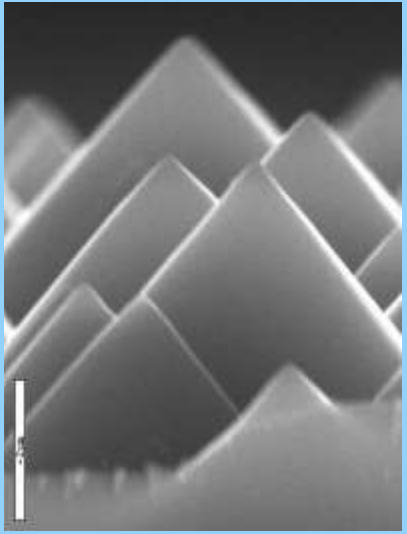
30 mm



Orientation (hkl)
10 %< R_{ref} <33 %

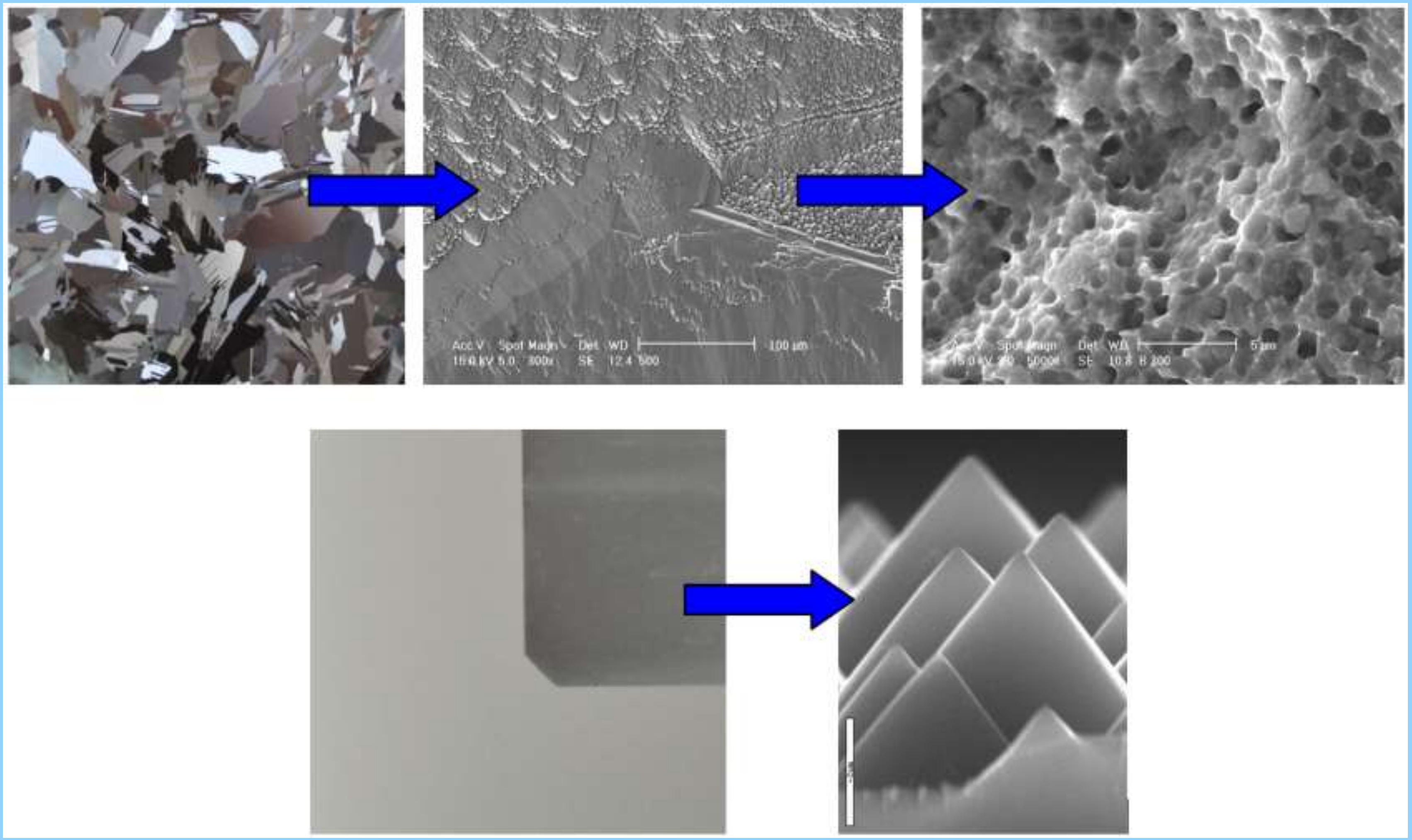
Orientation (111)
R_{ref} = 33 %

Orientation (100)
R_{ref} = 10 %

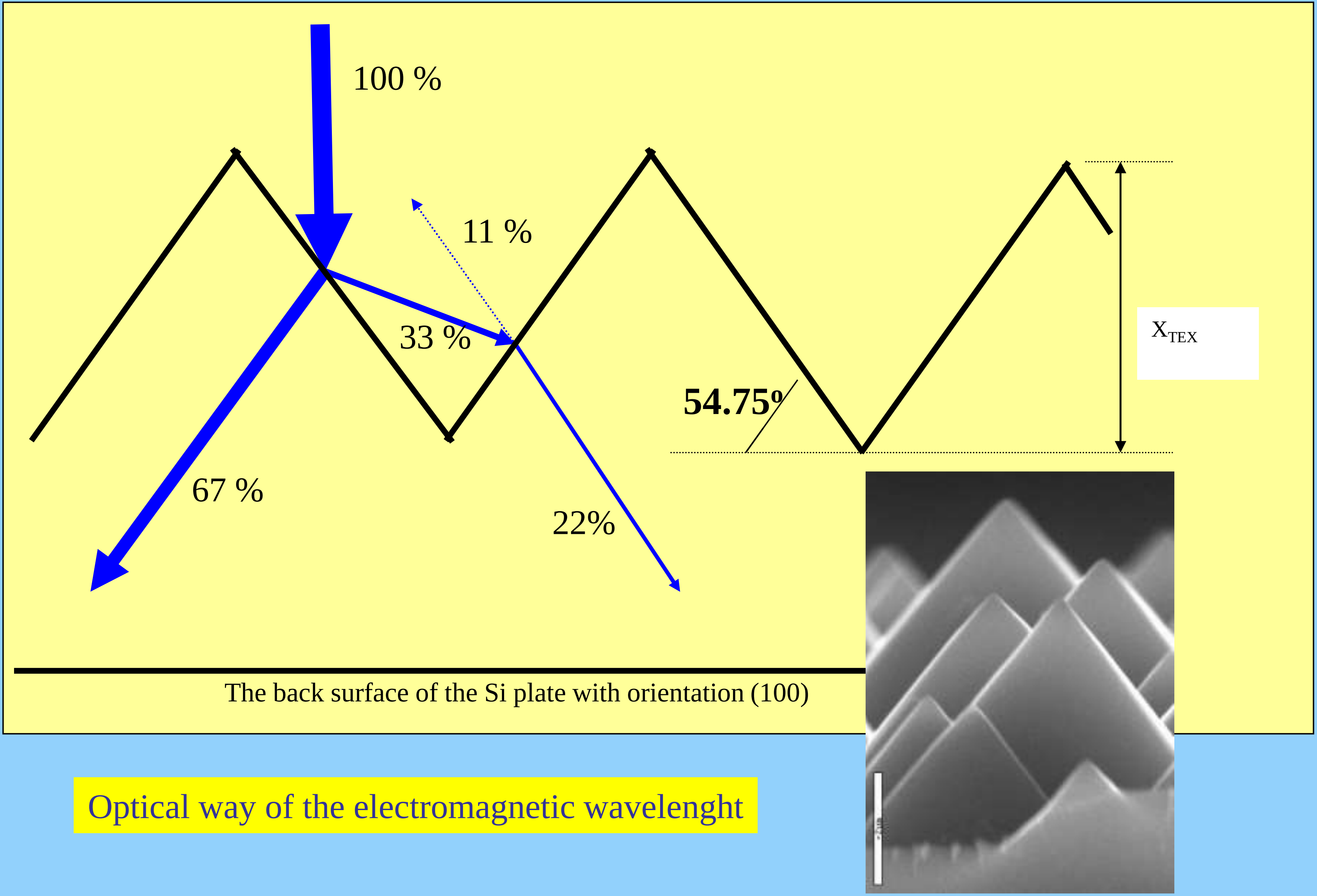


~ R_{ref} = 24 %

Texturization



Mc-Si silicon wafer, 25 cm^2 in surface area, after texturization in KOH solution, microphotograph of the area between grains, microphotograph of mc-Si after texturization in HF:HNO_3:H_2O, Cz-Si plate with crystallographic orientation (100) obtained from the producer, with a part of the surface texturized in KOH, microphotograph of texture (from left to bottom).



Optical way of the electromagnetic wavelenght

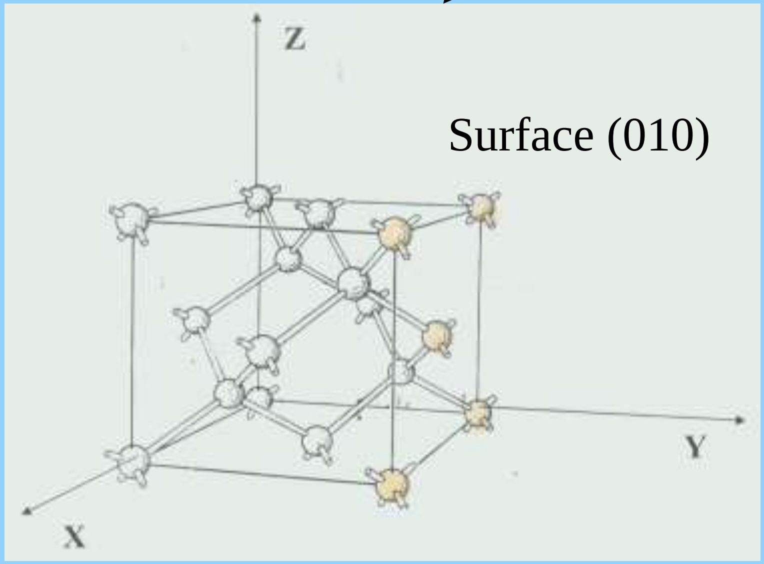
The silicon etching process in hydrooxides

$$Si + 2KOH + H_2O \rightarrow K_2SiO_3 + 2H_2$$

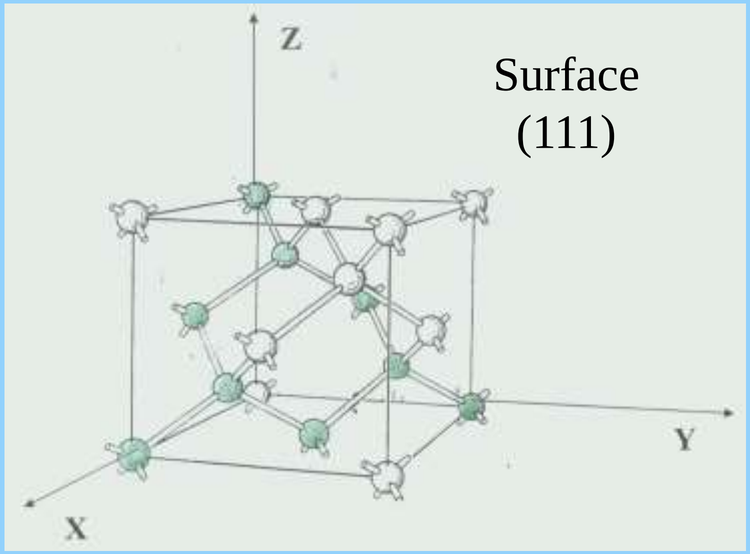
(at temperature 80 °C)

4 µm/min

0.4 µm/min



Surface (010)



Surface (111)

Methods of texturization of polycrystalline silicon surface applied in industry and research & development

No.	TEXTURIZATION METHOD	R_{eff} [%]	TEXTURE TYPE
1	Etching in NaOH or KOH solutions with photolithographic masking	~20	Reversed regular pyramids
2	Mechanical texturization with diamond saw	~5	Regular pyramids or grooves
3	Laser texturization	~10	Regular pyramids or grooves
4	Etching in HF-based acid solutions	~ 9	Sponge-type macro-porous layers
5	Electrochemical anodization in HF solutions	~10	Macro-porous layers
6	Plasma etching	~3	Irregular iglic-type pyramids
7	Etching in KOH and NaOH solutions without masking	~24	Regular and irregular geometric forms
8	Etching in HNO_3-HF solutions with photolithographic masking	~3	Regular honeycomb-form texture
9	Etching in plasma with additional etching in KOH solution	~21	Irregular pyramids

The chemical processes performed before producing the p-n junction aim at the elimination the **defected layer**, a formation of a **surface texture** which reduces the coefficient of reflection from the silicon surface, as well as the **cleaning of the surface** of all impurities and oxides. Thus prepared Si wafer is placed in the reactor of a diffusion furnace.

II Diffusion and p-n junction formation

The Si plates in the quartz holder are placed in a heated quartz reactor which is provided with protective gas N_2 and reactive gases $POCl_3$ and O_2. At the temperature above 800 ^{o}C, in the presence of oxygen, a dissolution of the $POCl_3$ occurs and, at the same time, phosphosilicate glass $xSiO_2 \cdot yP_2O_5$ (PSG) is formed on the Si surface, which further constitutes a local source of phosphorus diffusing in silicon. This process takes place according to the following dependences

$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2$$

$$2P_2O_5 + 5Si \rightarrow 5SiO_2 + 4P$$

Sources of the dopants

STEADY

Emulsion
Filmtronics509
(125 ml – 130 USD)

Paste
Filmtronics SPP-P600
(125 ml – 130 USD)

Paste P101
(500 ml – 100 EUR)

Plate BN

LIQUID

$POCL_3$ (250 ml - 500 zł)

BBr_3 (50 ml – 1000 zł)

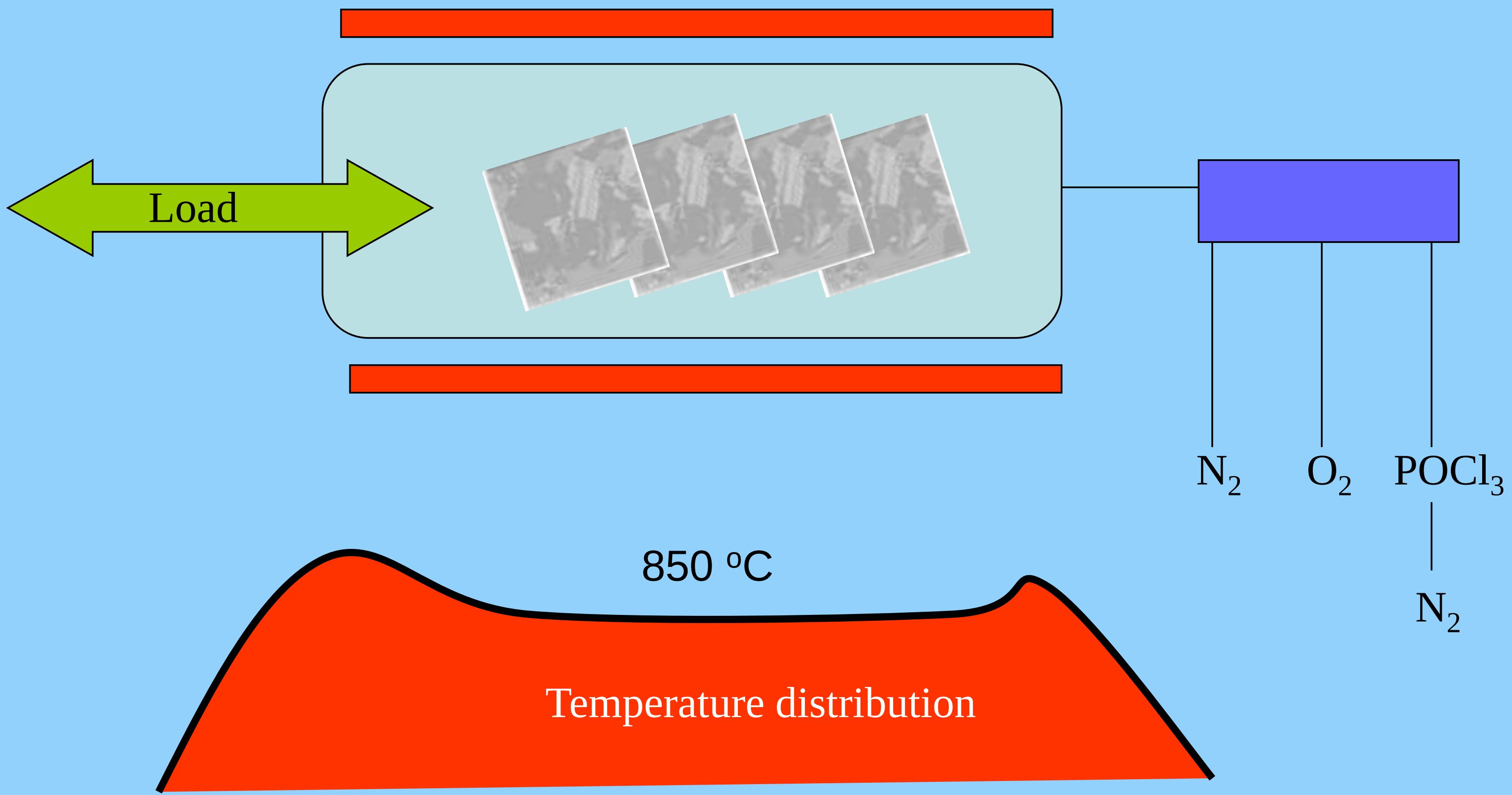
H_3PO_4

GASEOUS

10%BF_3 in N_2
(40 l – 7464 zł)

The industrial diffusion furnace

Quartz reactor



Load

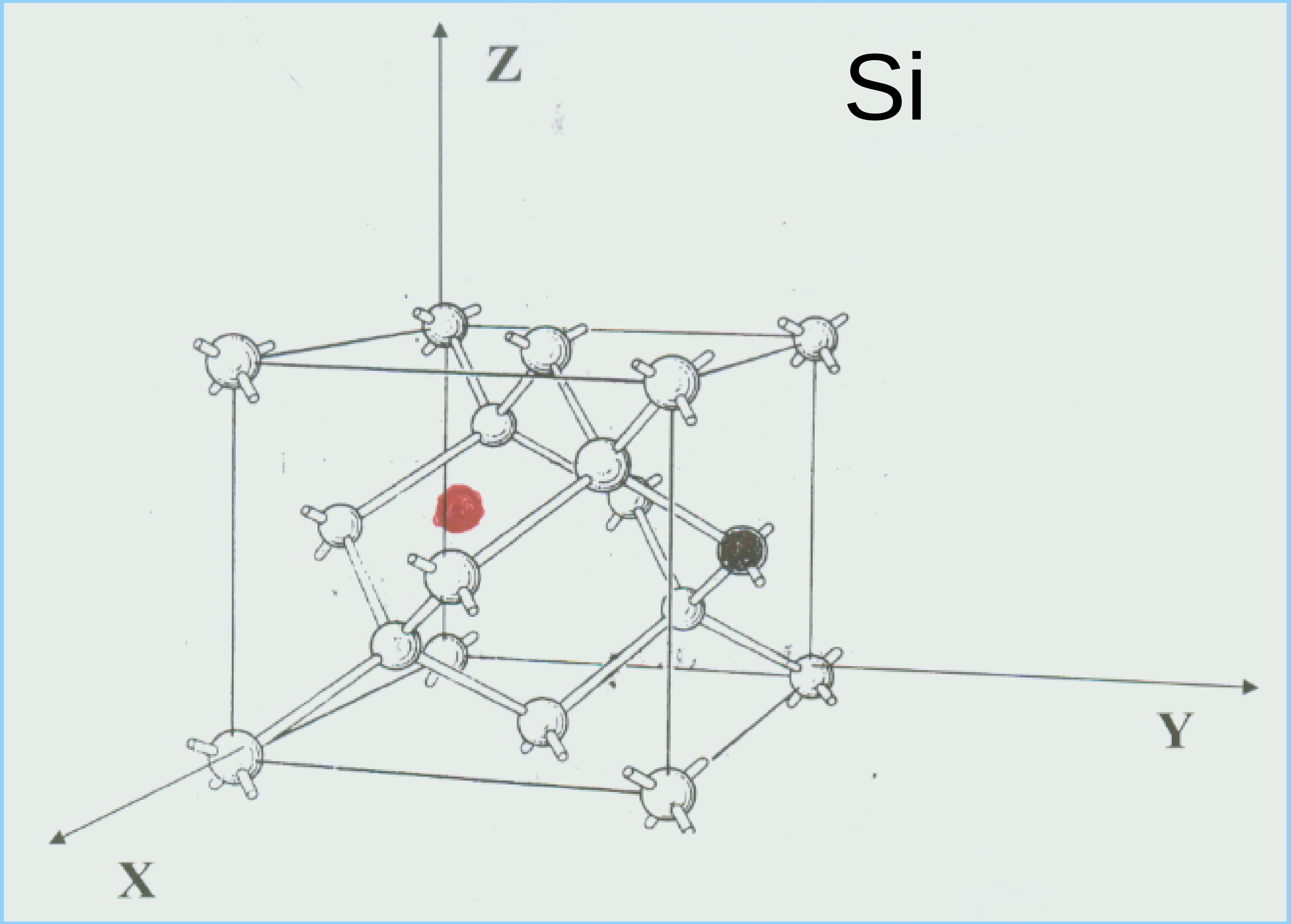
N_2 O_2 $POCl_3$

N_2

850 °C

Temperature distribution

During diffusion, the doping atmosphere must be supplemented with oxygen, so that the partial pressure P_2O_5 is sufficient to saturate PSG with phosphorus atoms. As a result of the diffusion process, some of the impurity atoms do not assume the substitution sites in the crystalline silicon structure, but instead they assume the interstitial sites, thus forming an electrically inactive layer, the, so called, dead layer. The concentration and the profile of the impurity are affected by the temperature, time and concentration of the reactive gases. The measurement of the layer resistance, performed with a four-point probe, is a control measurement after each diffusion process, which provides information not only on the value of Rρ but also on the homogeneity of the impurity distribution on the whole surface of the Si plate. Most of the producers currently perform doping of the n-type area with the value of Rρ at the level of 40 ÷ 50 Ω/□, where the fast development of paste production technologies and metallization processes of front electrode contacts makes it possible to produce a cell with the thick film technology for Rρ ~ 80 Ω/□.

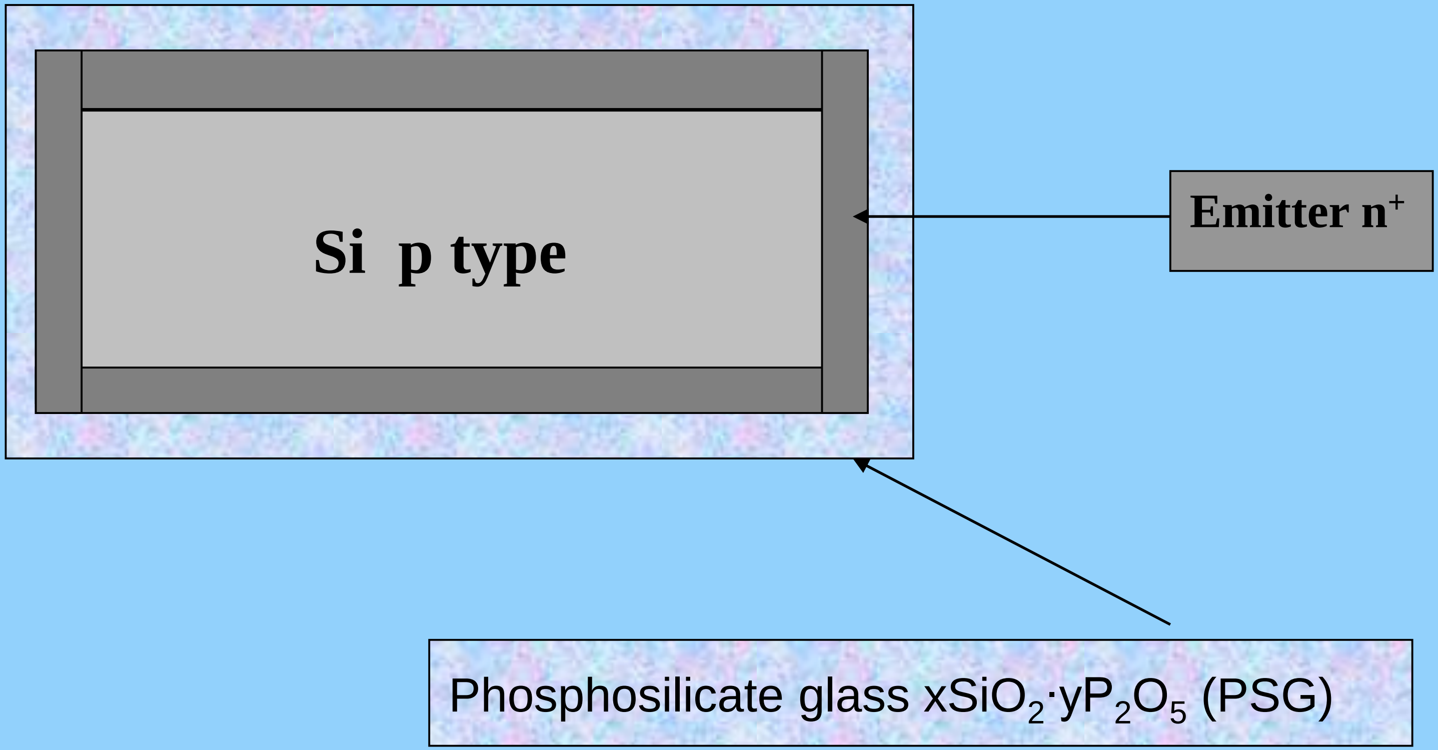


● - Dopant element in substitution position → **SR**

🔴 - Dopant element in interstitial position

← **SIMS**

In the diffusion process, the doping takes place on all sides of the plate.

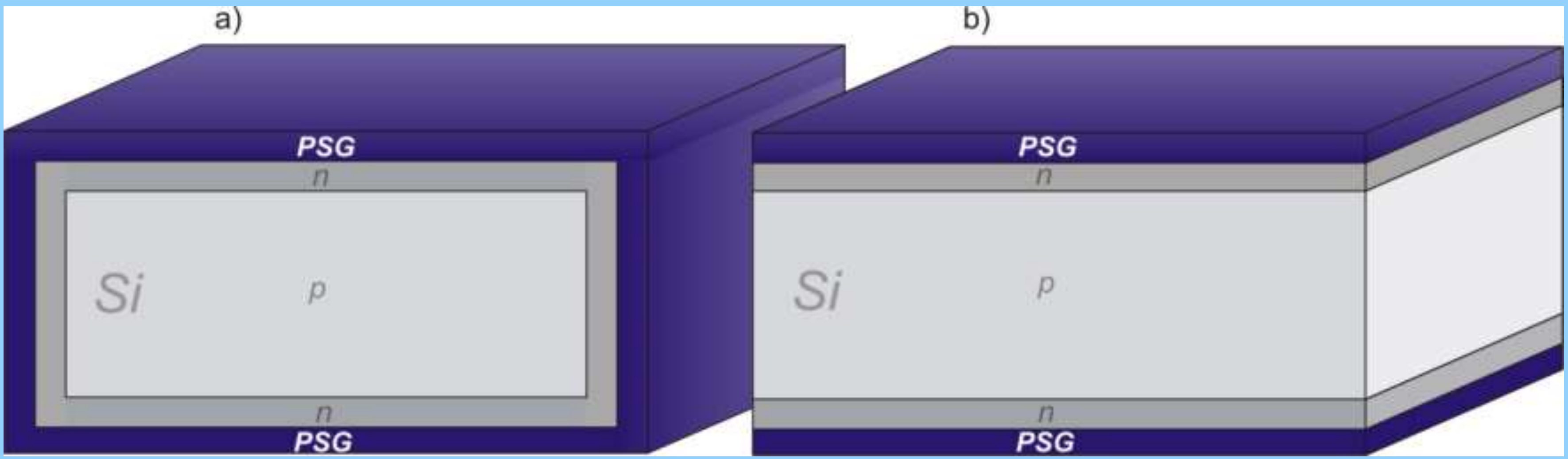


Si p type

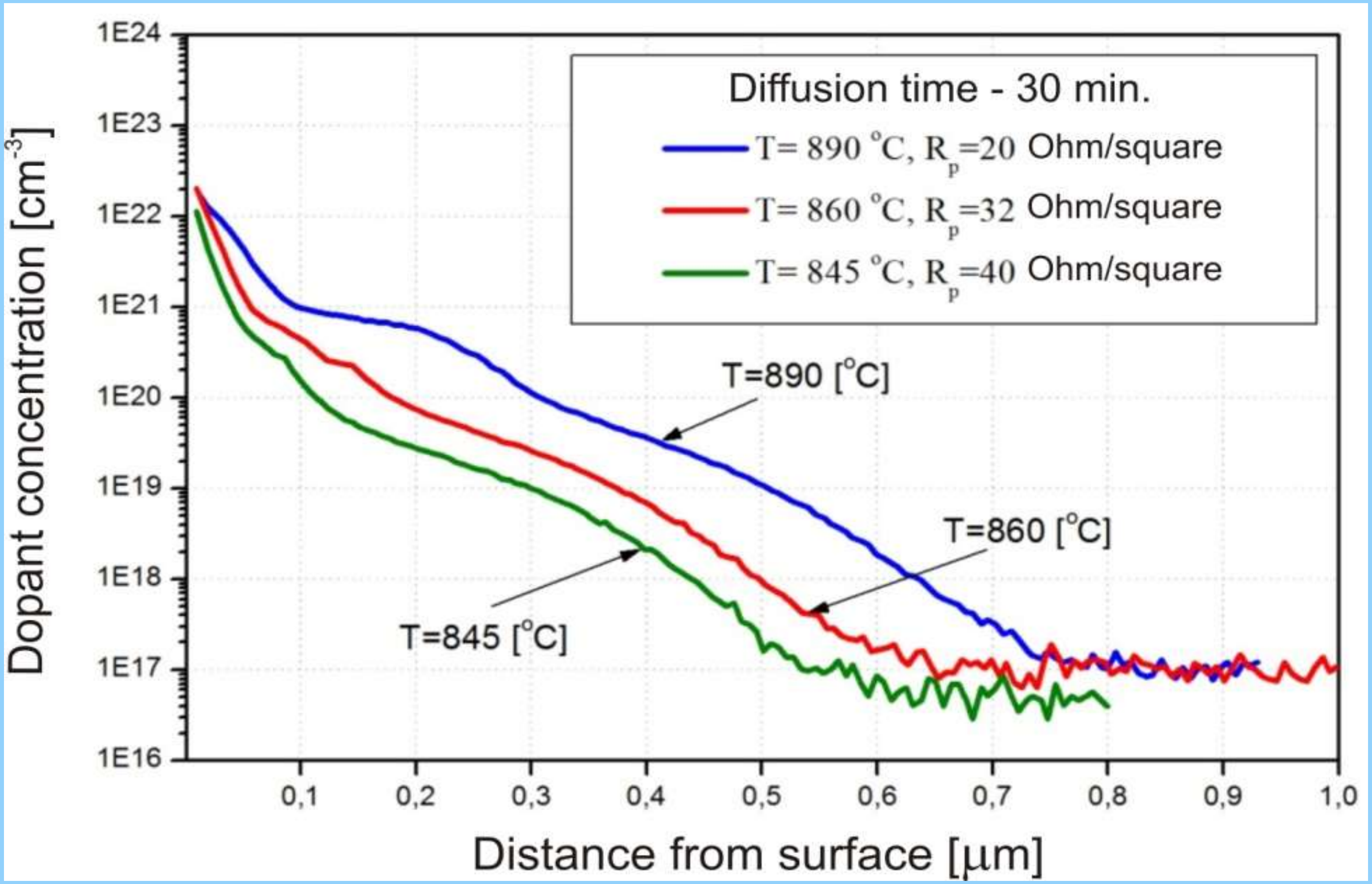
Emitter n^+

Phosphosilicate glass $xSiO_2 \cdot yP_2O_5$ (PSG)

The elimination of the short-circuit on the edges in the thick film technology is performed in the process of chemical etching of the edges, cutting the latter off with the use of laser or plasma etching.



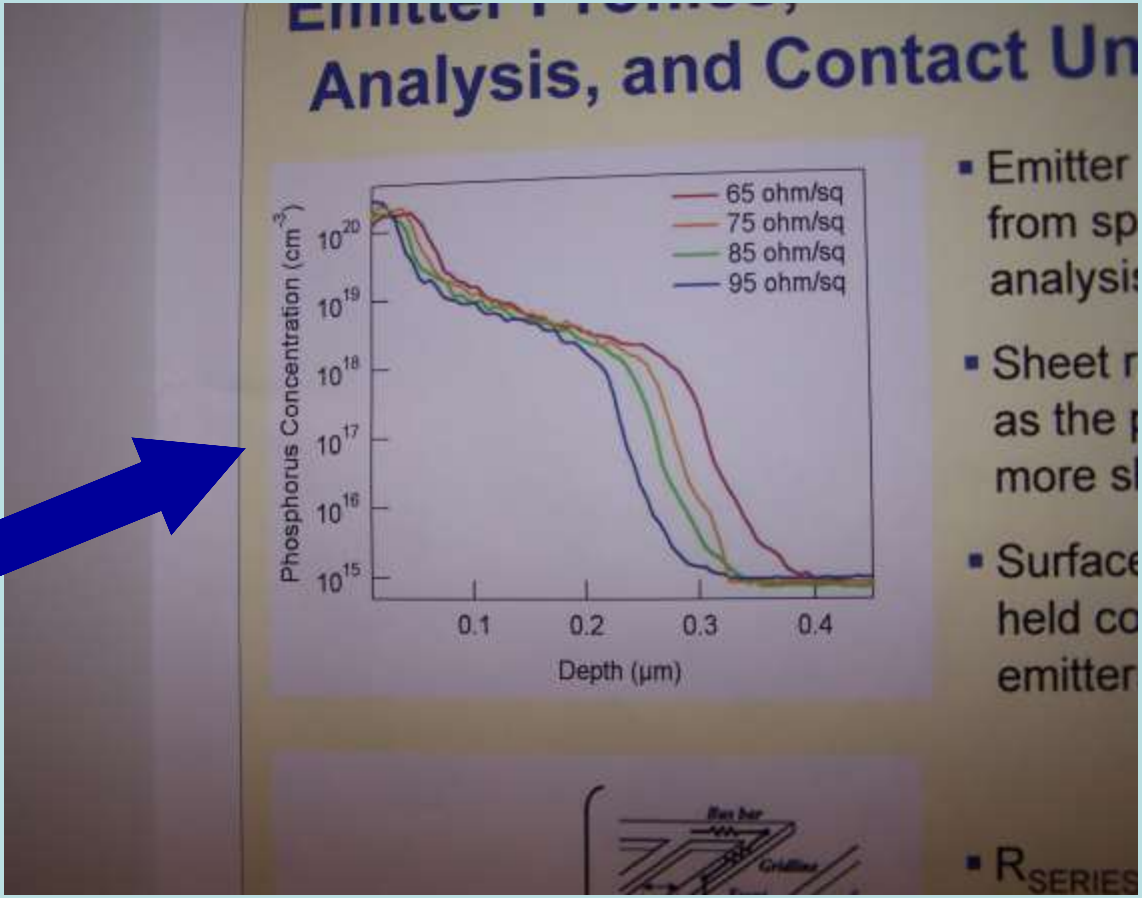
Cross-section of a plate after diffusion (a) and after edge separation (b)



Profiles of donor impurity distribution from source $POCl_3$ through secondary ion mass spectrometry (SIMS) at the Physics Institute PAN in Warszawa; together with the temperature value for the given diffusion process. The diagram also gives the surface resistance value Rρ of the donor impurity layer.

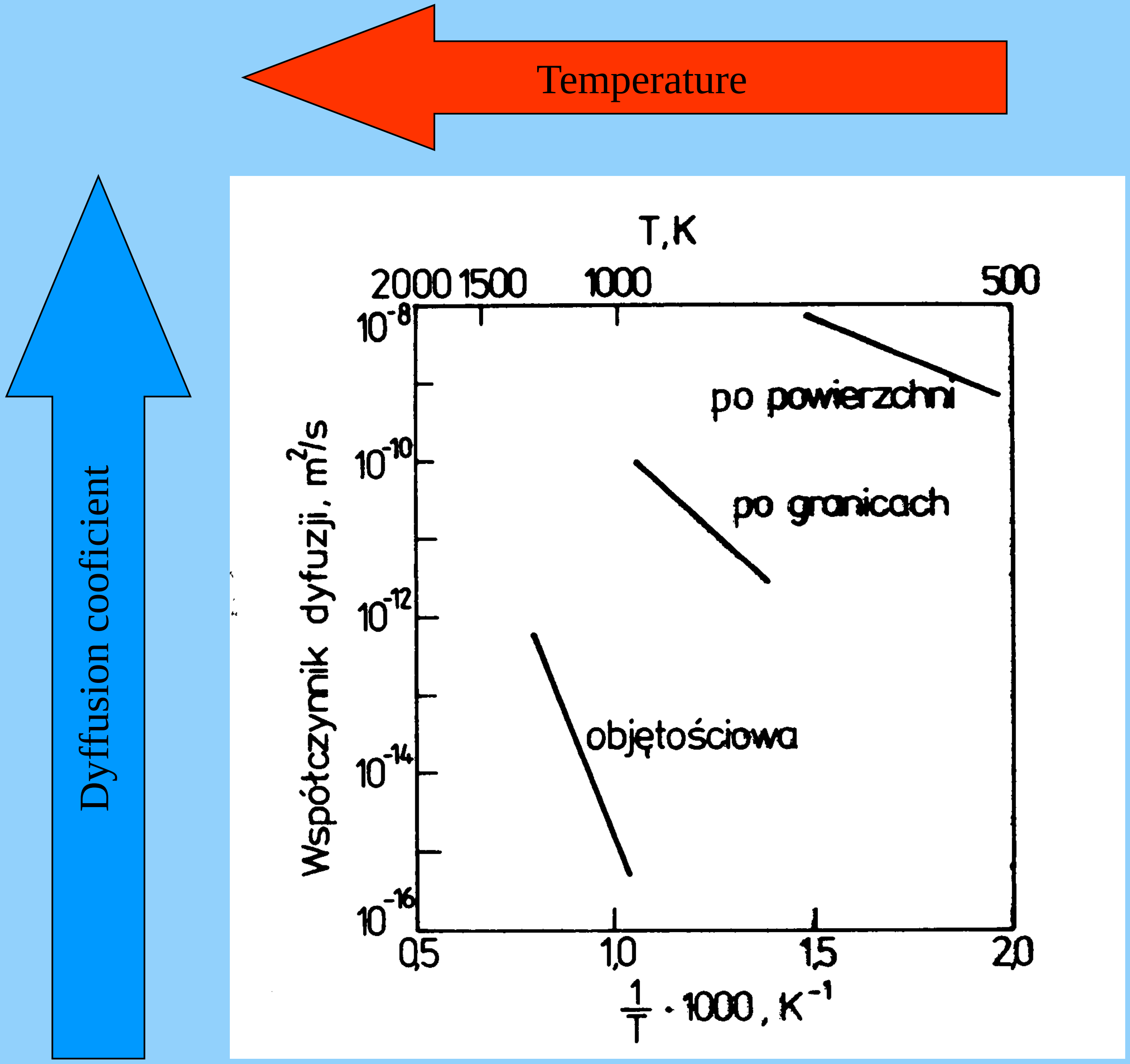
In-line diffusion process from H_3PO_4

In-line diffusion process - H_3PO_4



SIMS profiles after in-line diffusion

$x = \sim 0.3\ \mu m$

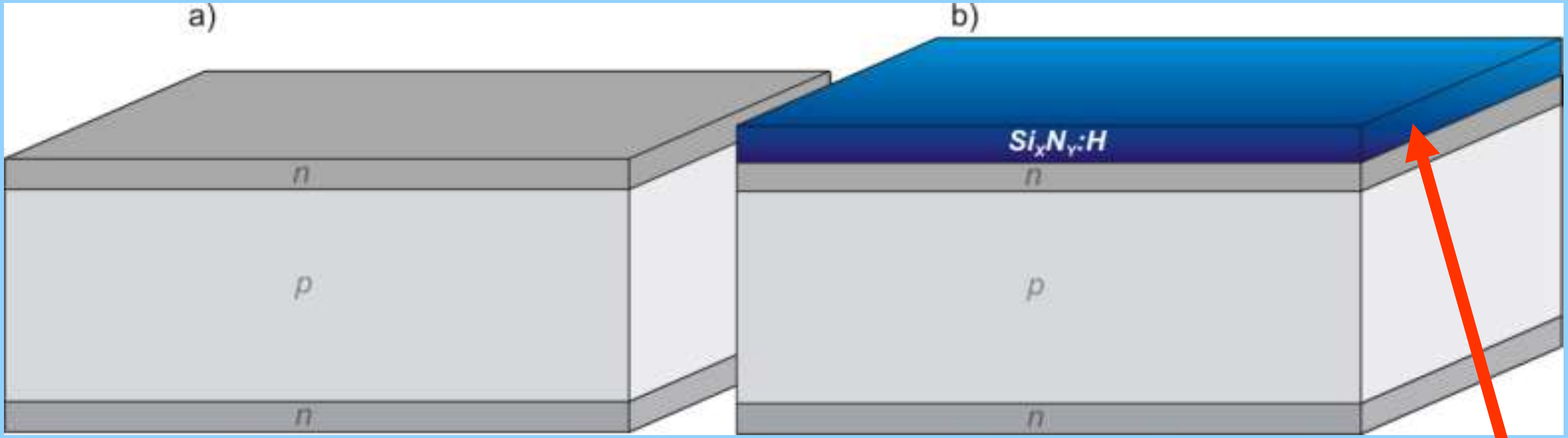


J. H. Brody, R. M. Rose, J. Wulff,
The strukture and properties of materials,
New York, John Wiley and Sons, 1964.
Z pozycji: M. Blicharski,
Wstęp do inżynierr materiałowej,
WNT Warszawa,2003, str.131.

III Deposition of passivation and antireflection coating

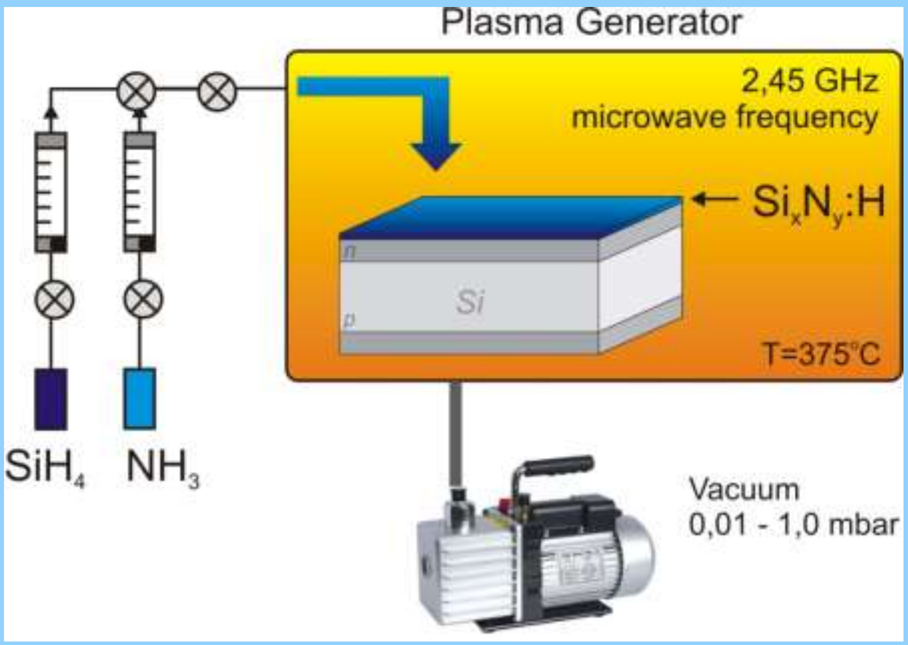
After separating the edge and eliminating the PSG glass layer in a 5% HF solution, a passivation and an antireflection coating (ARC) is deposited on the front surface of the plate. As the passivation coating, we can apply a SiO_2 layer, produced in dry oxygen at the temperature of 800 ^oC, and next, as the ARC coating, one can deposit e.g. a titanium oxide TiO_2 layer. The mass production of solar cells currently involves the application of only one layer which plays both functions, i.e. a coating of hydrogenated silicon nitride deposited with the method of RPECVD (Remote PECVD)

III Deposition of passivation and antireflection coating



Scheme of a plate section after the elimination of phosphosilicate glass (a) and after the deposition of a hydrogenated silicon nitride Si_xN_y:H (b)

The optimal Si_xN_y:H layer is of the thickness d ~ 85 nm and its refractive index has the value of n ~ 2,05. The above layer also has 10 ÷ 15 % at. H, and this hydrogen, in the process of contact metallization, passivizes the broken surface bondings, and in the case of m-Si – also the grain boundary areas



Scheme of the RPECVD method of deposition a $Si_xN_y:H$ layer formed as a result of decomposition of silane SiH_4 and ammonia NH_4, in which only the ammonia is decomposed into plasma, in the generator located outside the reaction chamber

The silicon nitride layer deposited by means of PECVD allows for a passivation of the Si surface, but at the same time, it plays the role of an antireflection coating. The Si_xN_y:H layer, due to its electron affinity, is appropriate for the n-type Si. In the case of the p-type Si surface, more suitable seems to be an Al_2O_3 layer, which is deposited with the method of ALD (Atomic Layer Deposition).

Layer type	Deposition method	SRV [cm/s]
SiO_2	Thermal	90
Si_xN_y:H	PECVD	10
Al_2O_3	ALD	70
a-Si:H	PECVD	30

Passivation coatings used in the silicon solar cell production and the surface recombination velocity (SRV) values obtained after applying the technology.

In high efficiency solar cells, the surface texturization is applied simultaneously with the ARC layer, which allows for a maximum reduction of R_{eff}. The ARC layer of the cell is required to fulfill a few basic conditions. One is to achieve the lowest possible value of the extinction coefficient k, which results in a high value of the transmission coefficient. As regards the value of the refractive index of the layer n_{arc} , it can be determined from the following relation:

$$n_{arc}d = \lambda_{opt}/4$$

where d is the thickness of the layer and λ_{opt} is the length of the wave for which the photon stream reaches its maximum

In the case of the silicon in which the refractive index n equals 3,87 for the wavelength of 632,8 nm, the optimal refractive index in the ARC layer equals 1,97

Refractive index n_{arc} in materials applied as ARC layers in silicon solar cells

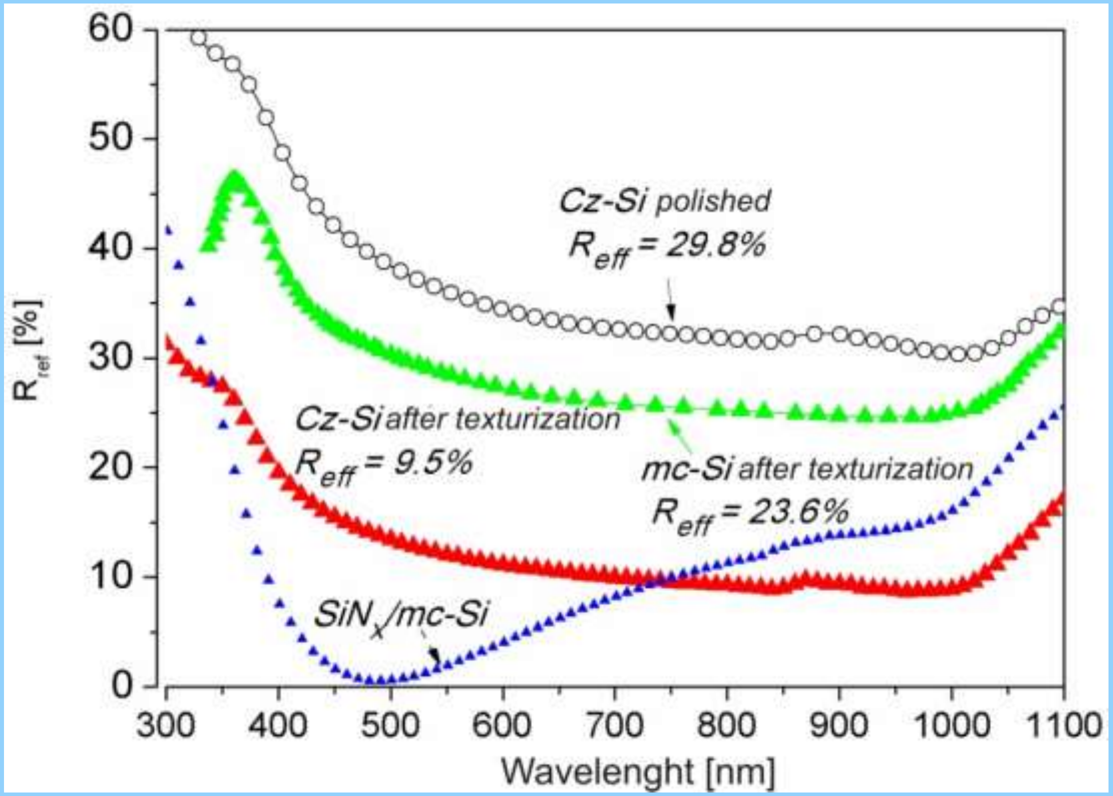
No.	MATERIAL	COATING METHOD	n_{arc}
1	MgF_2/ZnS	Vaccuum coating	1,38 / 2,34
2	MgF_2/CeO_2	Vapour deposition/ion sputtering for target Ce	1,38 / 2,47
3	SiO_2	Thermal oxidization	1,46
4	Si_3N_4	Gas phase deposition $SiH_4:H_2:NH_3$ in plasma	1,9 ÷ 2,3 1,9 ÷ 2,6
		High temperature gas phase deposition $NH_3:C_2H_6Cl_2Si$	1,55÷ 2,20
5	TiO_2	Hydrolysis with $Ti(OC_3H_7)_4$	2,38 ÷ 2,44
		Hydrolysis with $(C_2H_5O)_4Ti$	2,3 ÷ 2,5
6	$xSiO_2 \cdot yP_2O_5$	Gas phase deposition with $POCl_3$	1,71 ÷ 1,85
7	SnO_2	Hydrolysis with $SnCl_3$◌$5H_2O$	1,68
8	ZnO	Ion sputtering in atmosphere 1% O_2/Ar from target $ZnO:Al_2O_3$	1,9 ÷2,0

In order to precisely determine the effect of the ARC layer or the texture of the cell’s surface on the reduction of the radiation reflection, photovoltaics introduces a quantity described as the effective reflection coefficient R_{eff}. It is defined by the following formula:

$$R_{eff} = \int_{400}^{1100} R_{ref}(\lambda) N_{ph}(\lambda) d\lambda \;/\; \int_{400}^{1100} N_{ph}(\lambda) d\lambda$$

$N_{ph}(\lambda)$ – the number of photons falling on a surface unit for a given wavelength per one second for solar spectrum AM1.5

Texturization + ARC



Dependence of the reflection coefficient on the wavelength for surface-polished silicon Cz-Si and mc-Si, after texturization and deposition of a silicon nitride ARC layer; measurements performed with a spectrophotometer Perkin-Elmer Lambda-19, at AGH, Krakow.

Surface recombination velocity

Solar cells differ from other electron devices in a much larger surface, which makes the latter's effect on the cell parameters highly significant. Breaking the crystal's periodicity on the surface and the existence of unsaturated bonds causes the appearance of additional acceptor energy levels localized in the silicon's energy gap. On the real Si surface, coated with a thin layer of natural oxide, one can find acceptor, donor and trapping states. The effect of the surface on the kinetics of the electron processes is described by a quantity called surface recombination velocity S, defined as:

$$S = \frac{J_r}{q \cdot \Delta n_e} = \sigma_r \upsilon_r N_r$$

where:

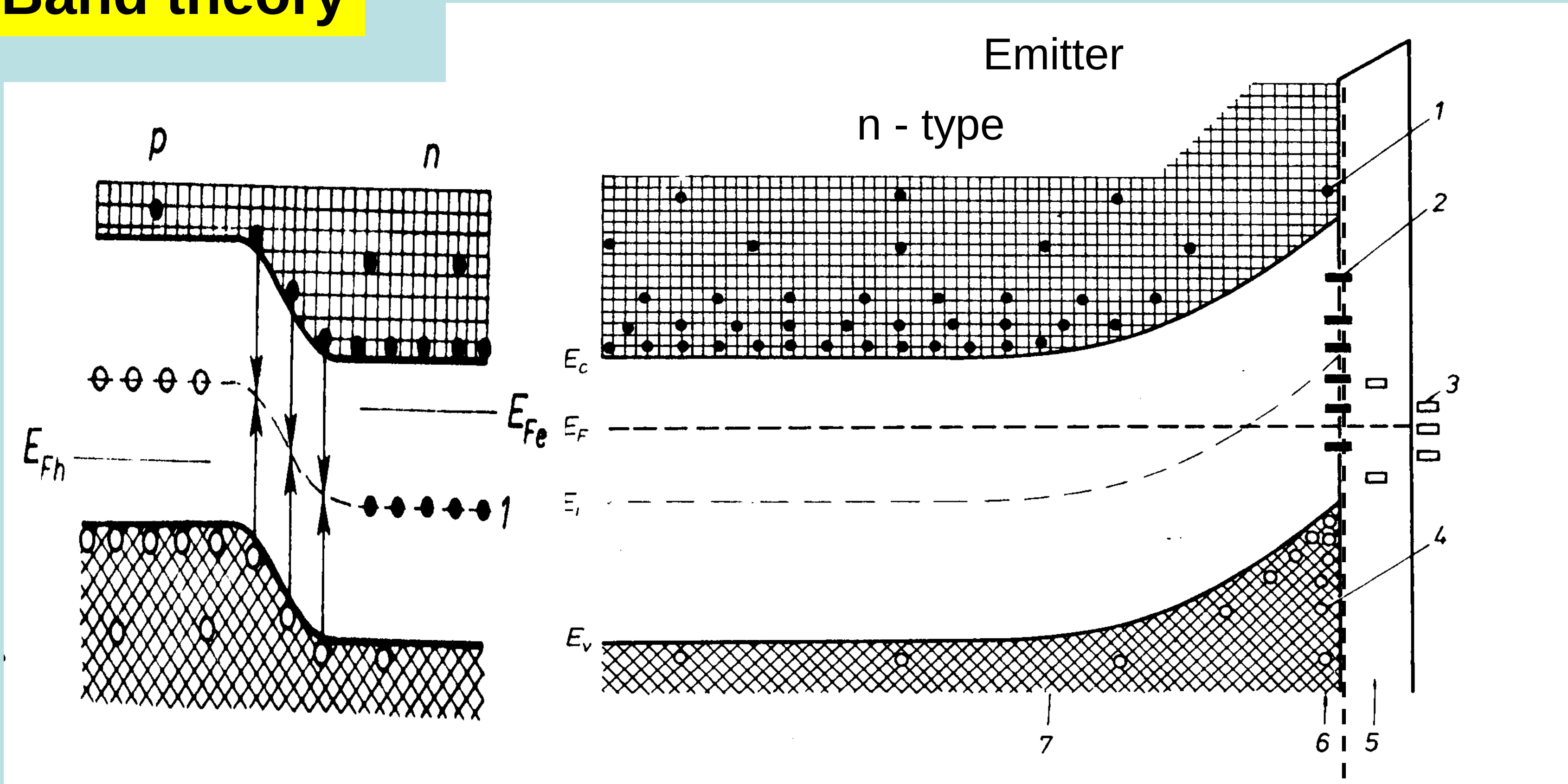
J_r – density of the electron or hole current flowing to the surface, for maintaining the established state in which the excess charge carrier concentration in the volume equals Δn_e,

N_r – number of recombination centres per surface unit,

σ_r – collision cross-section of charge carrier capturing,

υ_r – thermal velocity of charge carriers

Band theory



1 – electron, 2 – fast state, 3 – slow state, 4 – hole,
5 – oxide, 6 – inversion layer, 7 – Si n type

Surface of the Si plate

Physical dimension of the SRV

$$S = \frac{J_r}{q \cdot \Delta n_e} = \sigma_r \upsilon_r N_r$$

$$[S] = \frac{\mathrm{A/cm^2}}{\mathrm{C} \cdot \mathrm{1/cm^3}} = \frac{\mathrm{A/cm^2}}{\mathrm{A} \cdot \mathrm{s} \cdot \mathrm{1/cm^3}}$$

cm / s

100 cm/s

100000 cm/s

where:

J_r – density of the electron or hole current flowing to the surface, for maintaining the established state in which the excess charge carrier concentration in the volume equals Δn_e,

N_r – number of recombination centres per surface unit,

σ_r – collision cross-section of charge carrier capturing,

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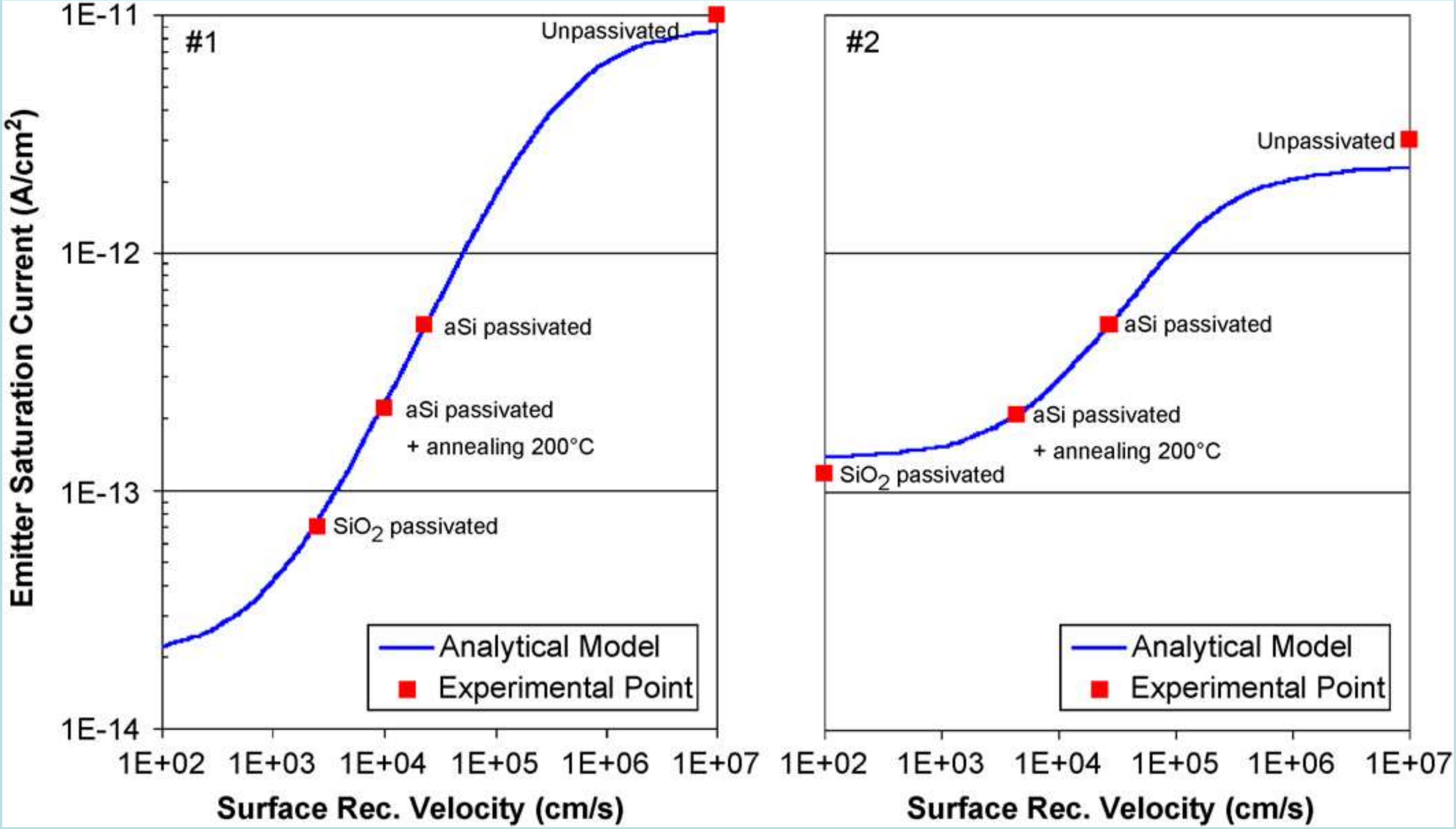
Layer type	Deposition method	SRV [cm/s]
SiO_2	Thermal	90
Si_xN_y:H	PECVD	10
Al_2O_3	ALD	70
a-Si:H	PECVD	30

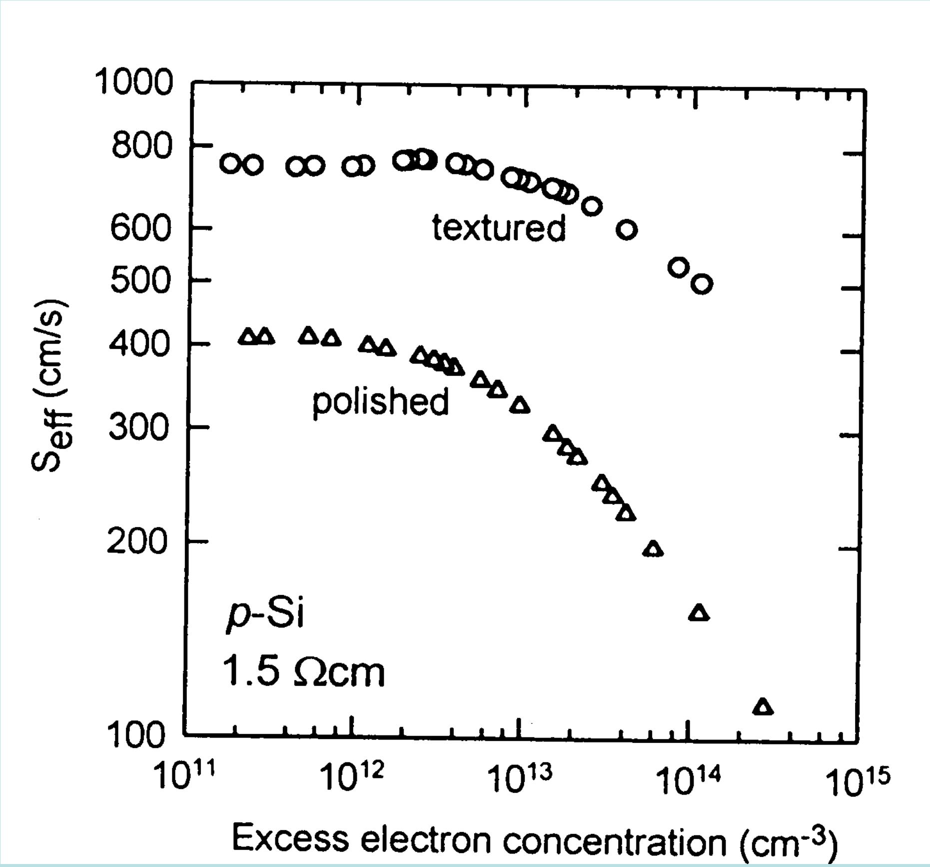
Effect of passivation on surface recombination velocity

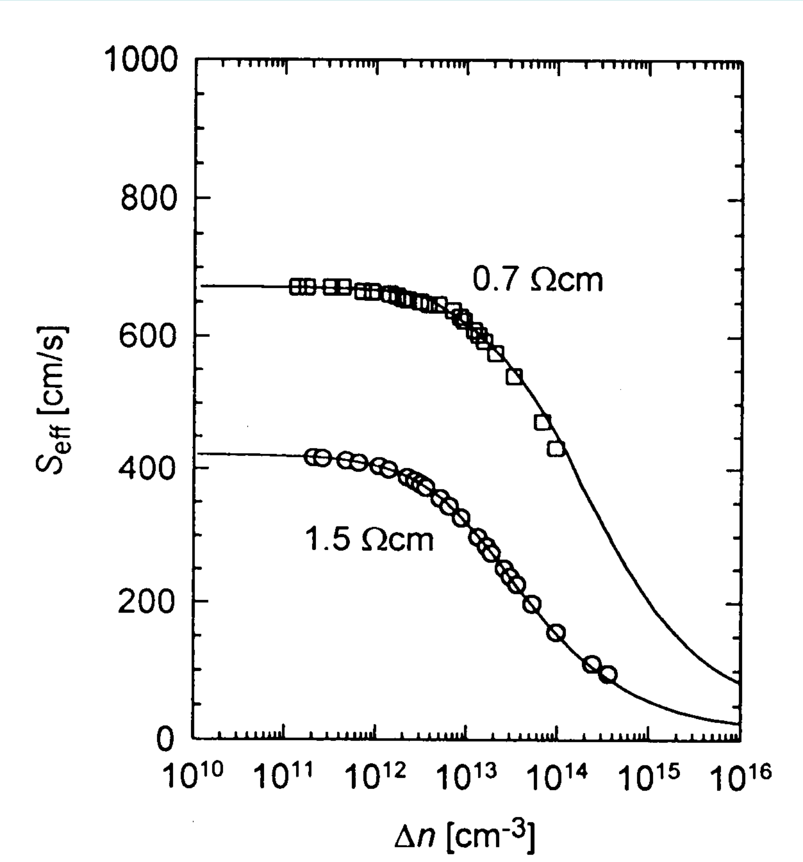
100 ohm/sq

40 ohm/sq



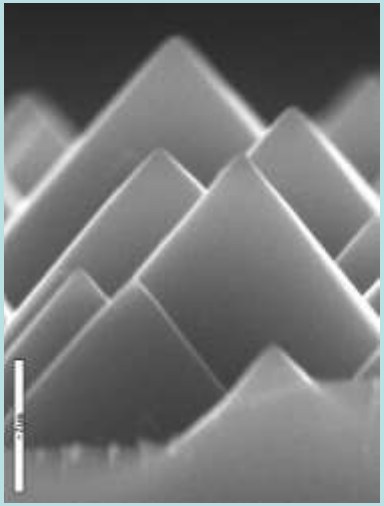
Influence of surface conditions on the properties of passivating oxide layer



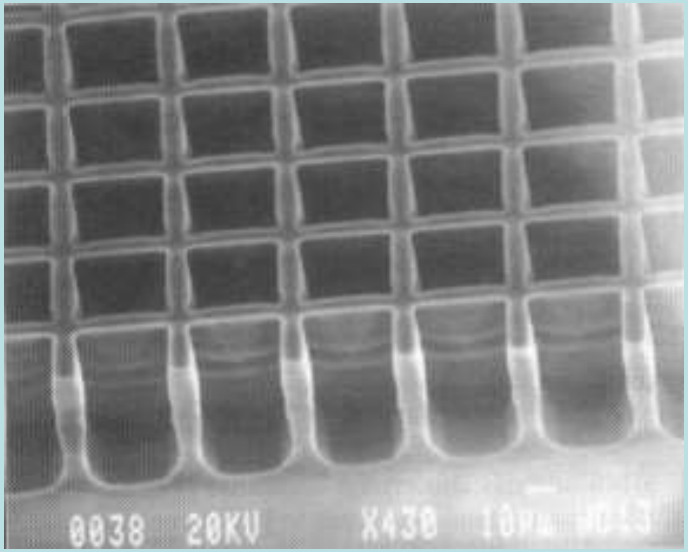


A. G. Aberle, „Solar Cells”, Bloxham and Chambers, Australia, 1999

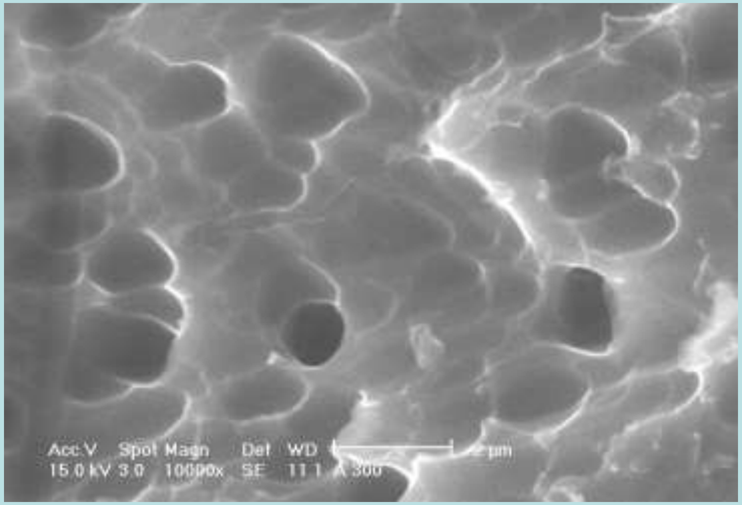
Surface development depending on texturization process



Etched in
KOH soluton



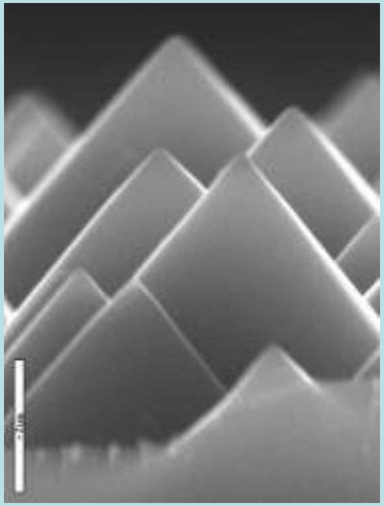
Si n type (100), photolitography



Etched in
$HF:HNO_3:H_2O$

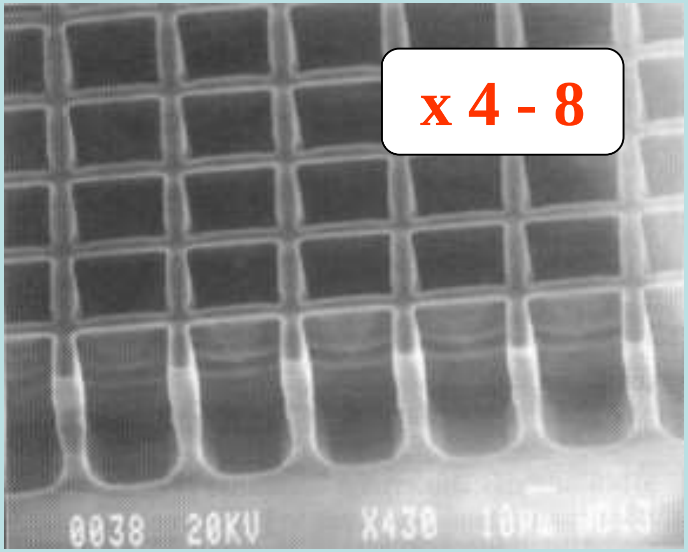
A.Fave, B. Semmache, S. Berger, P. Kleiman, F. Mazel, Ch. Dubois, J. M. Olchowik, A. Laugier, “Direct LPE Growth of Textured Silicon Thin Layers on C-Si Etched-Grid Fixed on Ceramic Substrate”, Proc. of the 16th European Photovoltaic Solar Energy Conference, 1-5 May, 2000, Glasgow, 1140-1143.

Surface development depending on texturization process



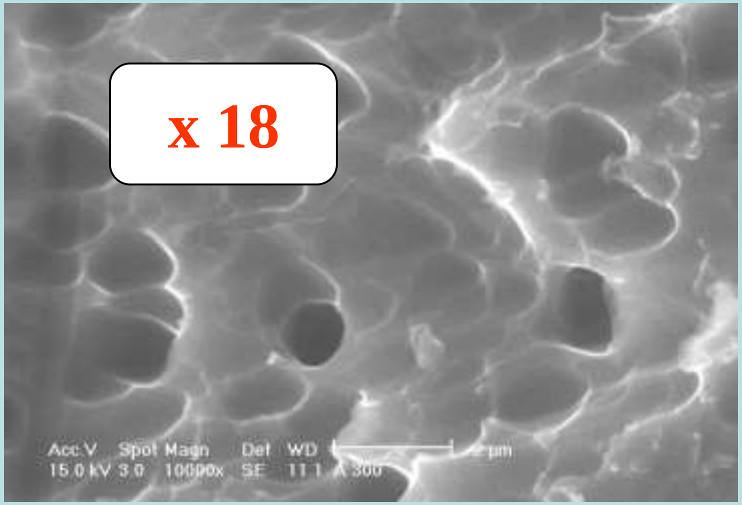
x 1.7

Etched in
KOH
solution



x 4 - 8

Si n type (100), photolitography



x 18

Etched in
$HF:HNO_3:H_2O$

A.Fave, B. Semmache, S. Berger, P. Kleiman, F. Mazel, Ch. Dubois, J. M. Olchowik, A. Laugier, "Direct LPE Growth of Textured Silicon Thin Layers on C-Si Etched-Grid Fixed on Ceramic Substrate", Proc. of the 16th European Photovoltaic Solar Energy Conference, 1-5 May, 2000, Glasgow, 1140-1143.

$$1/\tau = 1/\tau_B + 1/\tau_E + 1/\tau_{SB} + 1/\tau_{SF}$$

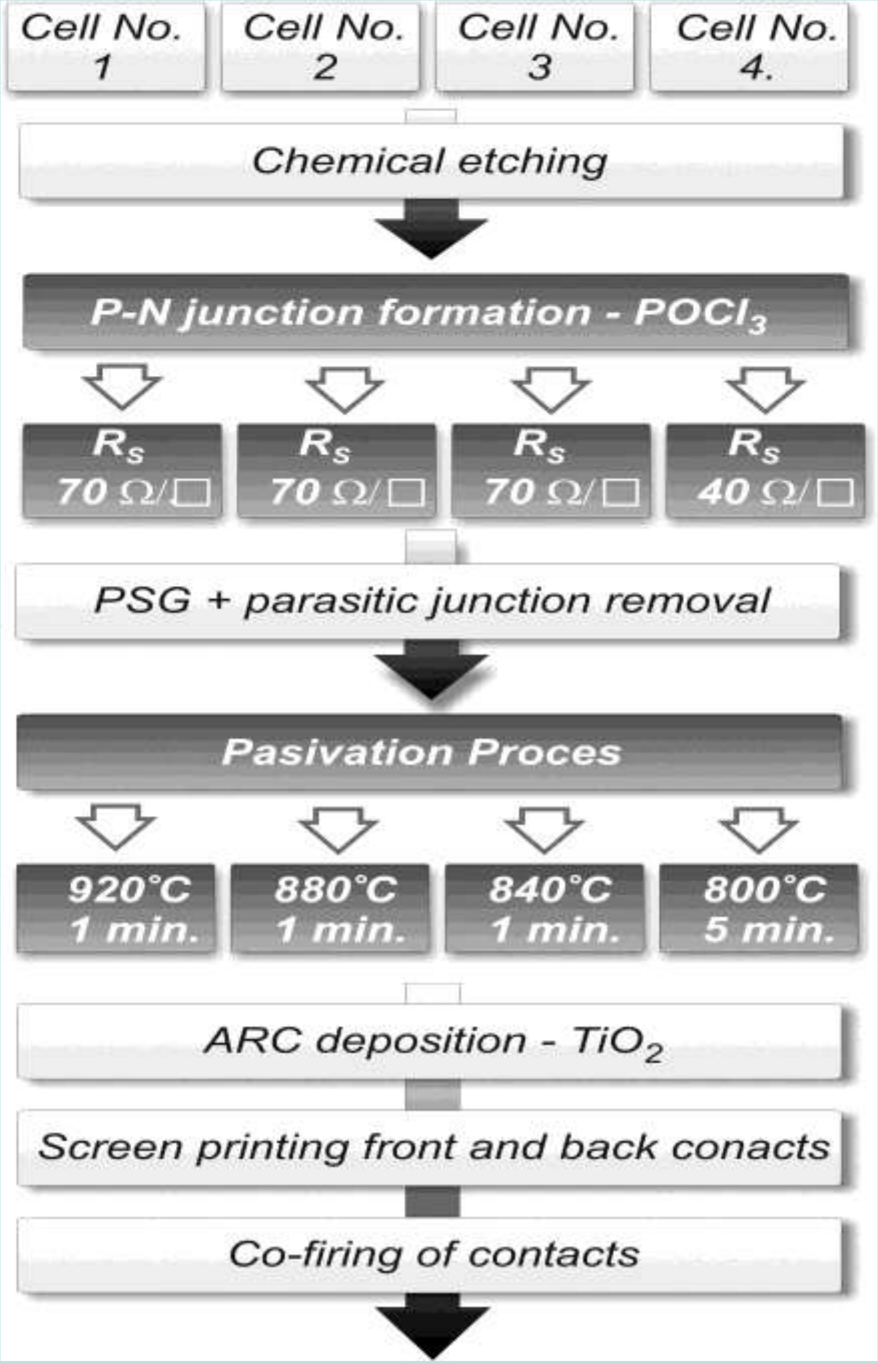
WCT Sinton Con. Inc.

The effective lifetime dependence on a type of Si and sheet resistance after diffusion process

$$1/\tau = 1/\tau_{B} + 1/\tau_{E} + 1/\tau_{SB} + 1/\tau_{SF}$$

Type Si	Before diffusion process τ [μs]	After diffusion $R_{sheet} = 36\ \Omega/\square$ τ [μs]	After diffusion $R_{sheet} = 58\ \Omega/\square$ τ [μs]
Cz-Si	**3.6**	**14.1**	**17.1**
mc-Si	**2.1**	**11.2**	**13.0**

Different passivation temperatures



Cell No. 1 | Cell No. 2 | Cell No. 3 | Cell No. 4.

Chemical etching

P-N junction formation - $POCl_3$

R_s 70 Ω/□	R_s 70 Ω/□	R_s 70 Ω/□	R_s 40 Ω/□

PSG + parasitic junction removal

Pasivation Proces

920°C 1 min.	880°C 1 min.	840°C 1 min.	800°C 5 min.

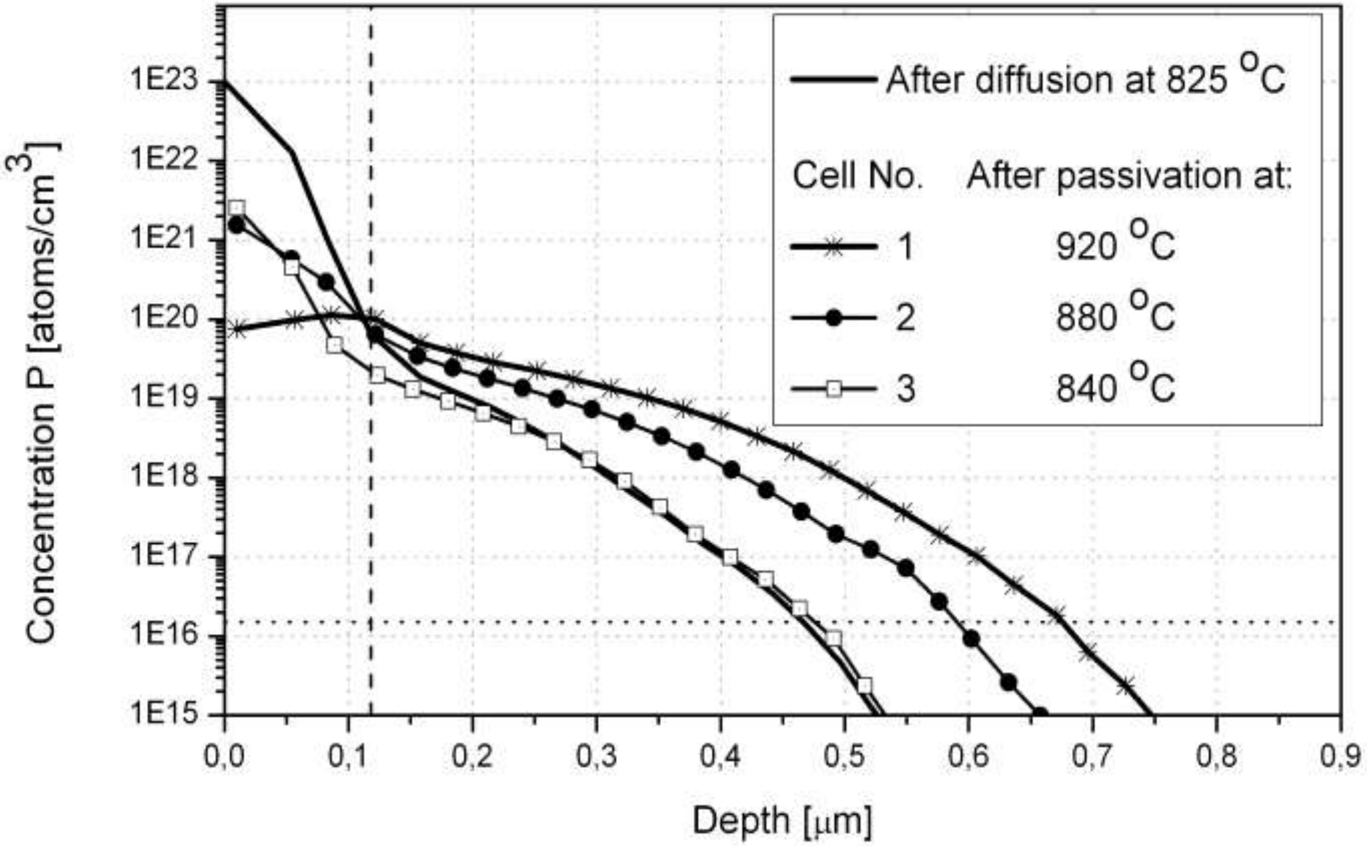
ARC deposition - TiO_2

Screen printing front and back conacts

Co-firing of contacts

Infuluence of the process temperature on the dopant profile

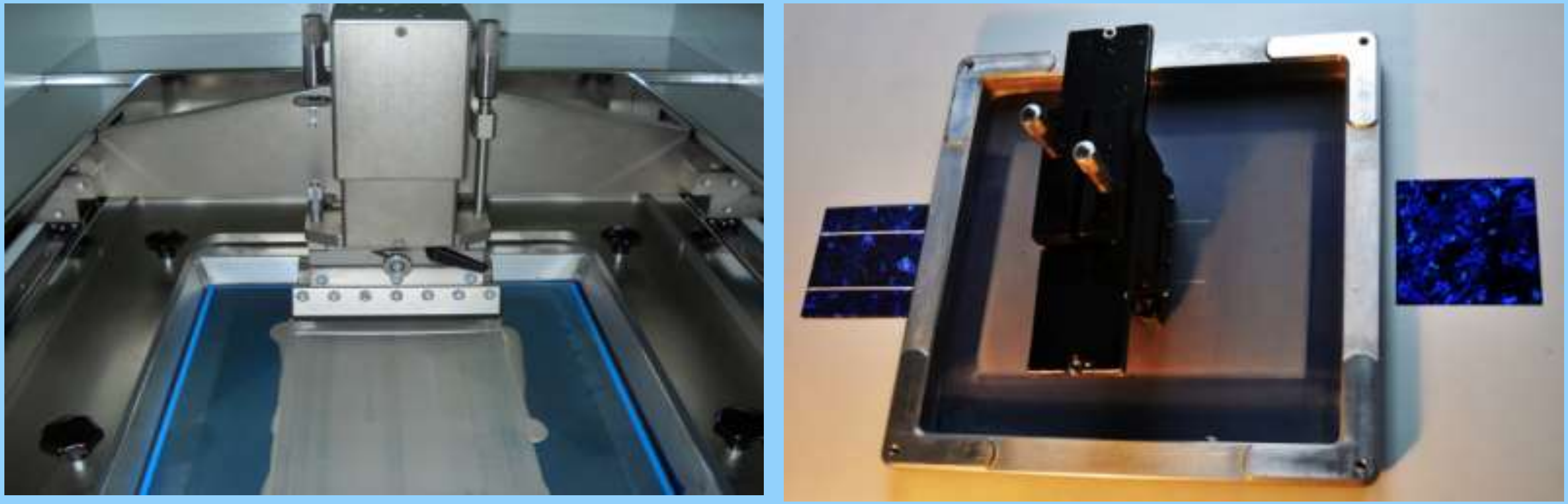
passivation process



IV Screen printing process deposition of front and back electrode of the cell

In order to create electrical contacts of the cell, its front and rear surface is coated with pastes with the screen process method. The biggest producer of pastes applied in photovoltaics is currently Du Pont. The determined scheme of the deposited paste is the image of a pattern existing on a steel sieve, usually of the density of 280 ÷ 320 msh, where the number of msh denotes the number of the sieve meshes for a distance of 1 inch. The width of the front collecting electrode usually equals 2 mm, and in the case of thin collecting electrodes, this value is from 80 to 120 μm, with a parallel spacing every 2,7 mm. The width and the spacing of the paths is a compromise between the minimization of the component R4 of the cell's series resistance and the surface area of the cell's front side's coverage with electrodes, the, so called, cover coefficient - 5 %. After the deposition of paste on the given side of the plate, the latter is dried at the temperature of 150 ^{o}C, for 15 minutes, and this process is repeated on the opposite side. The rear surface of the cell is additionally covered with an Ag + 2 % Al strip, which allows for a solder seal, which is not possible in the case of the Al layer covering the remaining part of the surface.

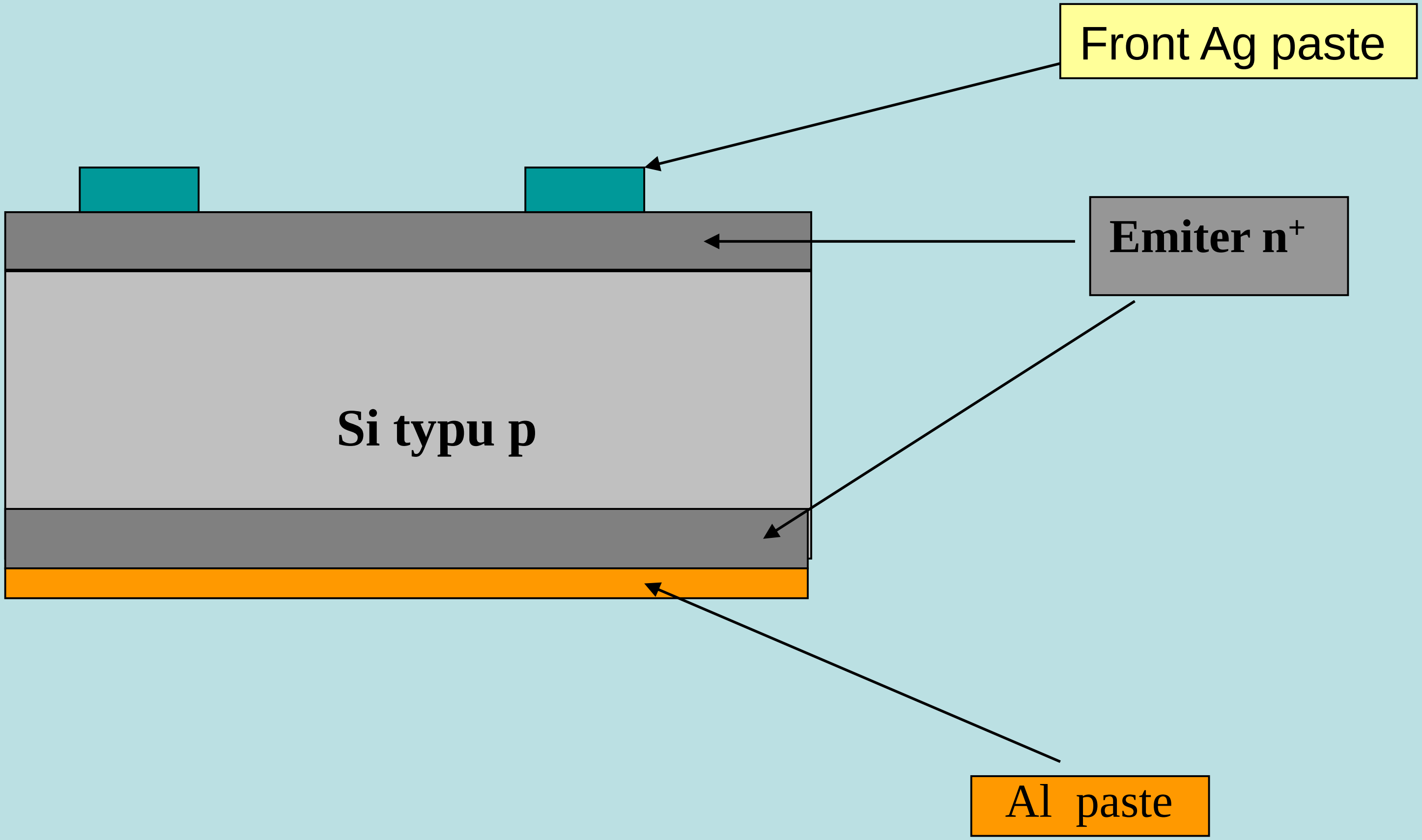
Screen-printing



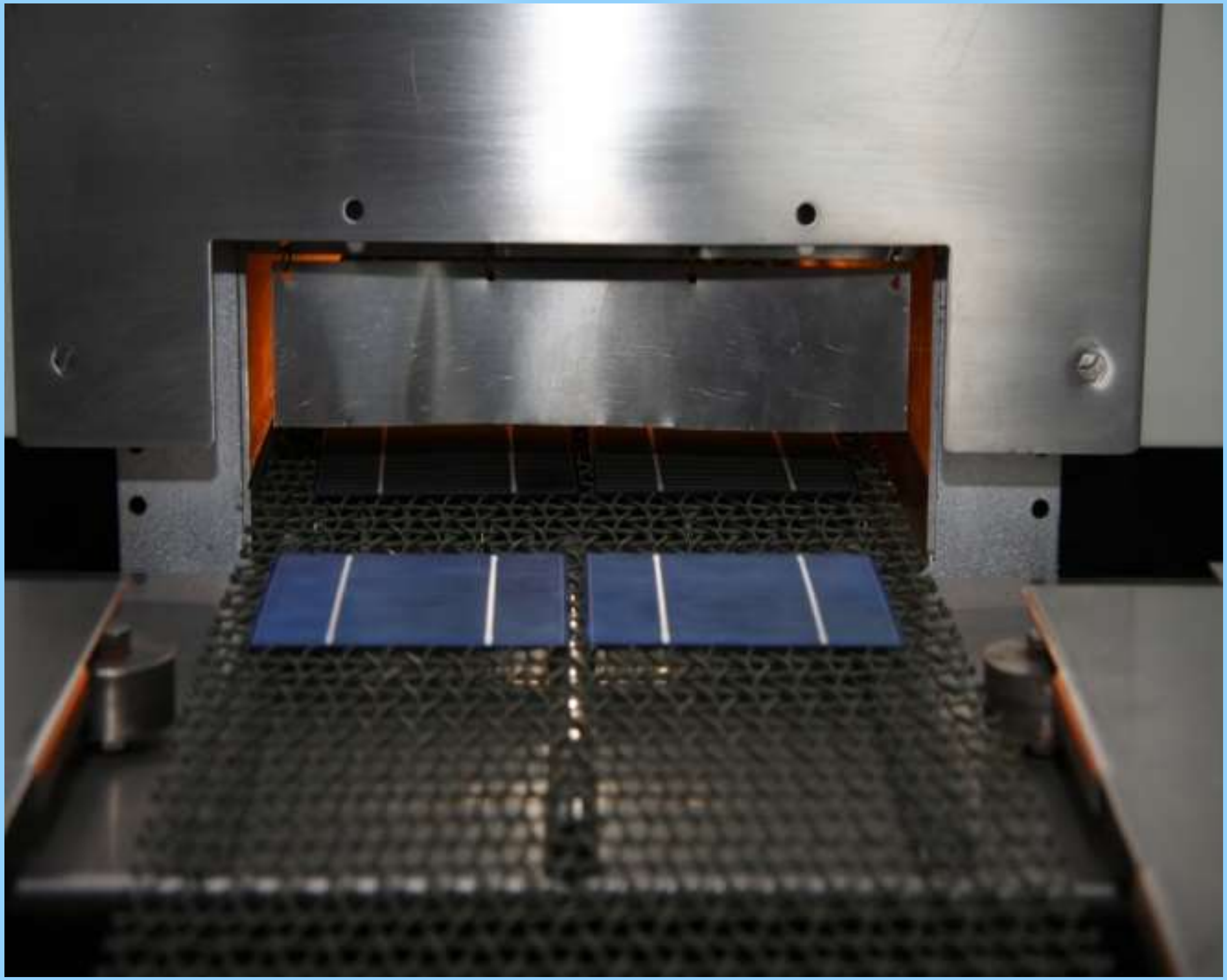
System of squeegees brushing the paste over the sieve and pressing the paste through the meshes onto the plate’s surface (left) and a sequence of paste printing in the process of creating the front electrode with the screen process method (right)

Screen-printing

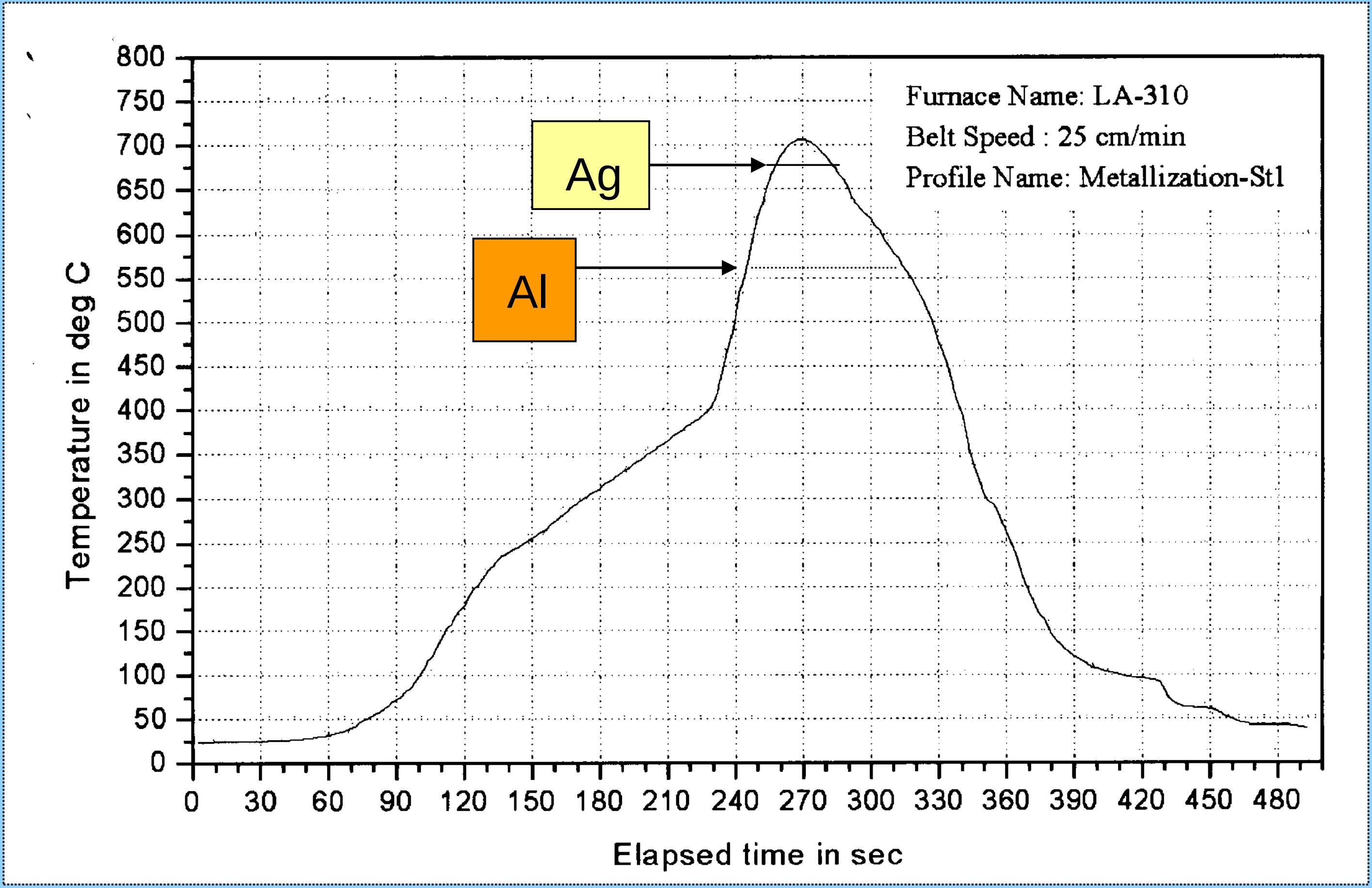
Scheme of solar cell section after screen-printing process



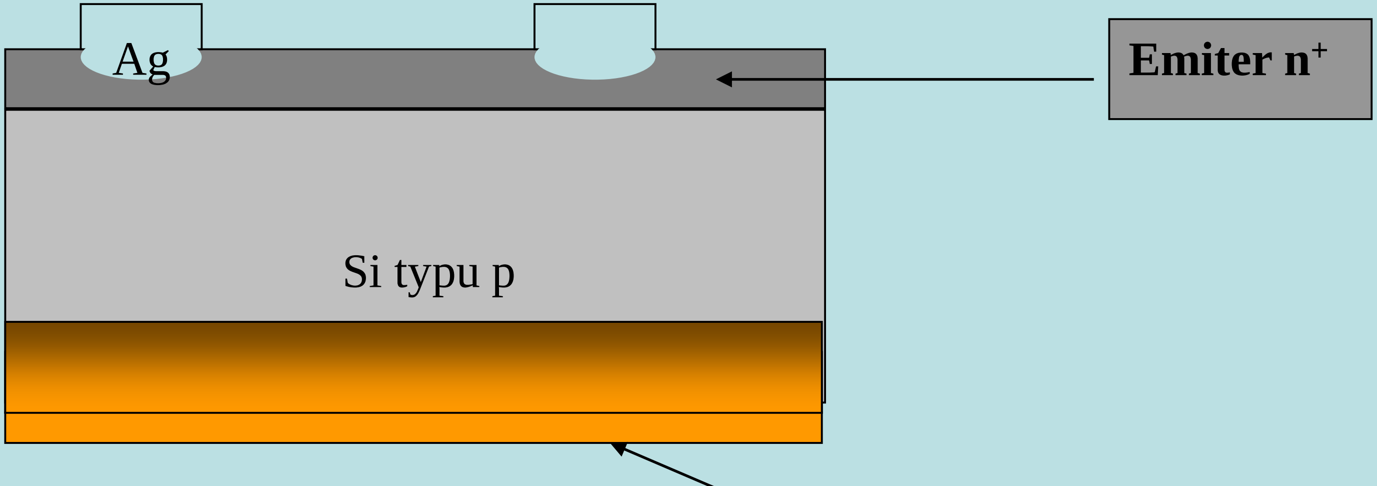
Metallization process



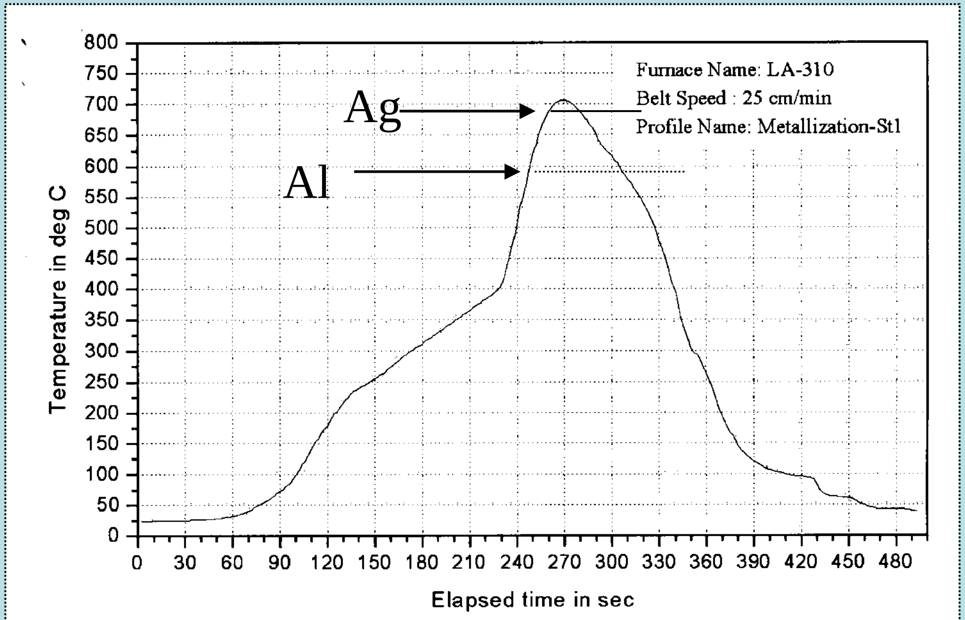
Temperature at IR furnace



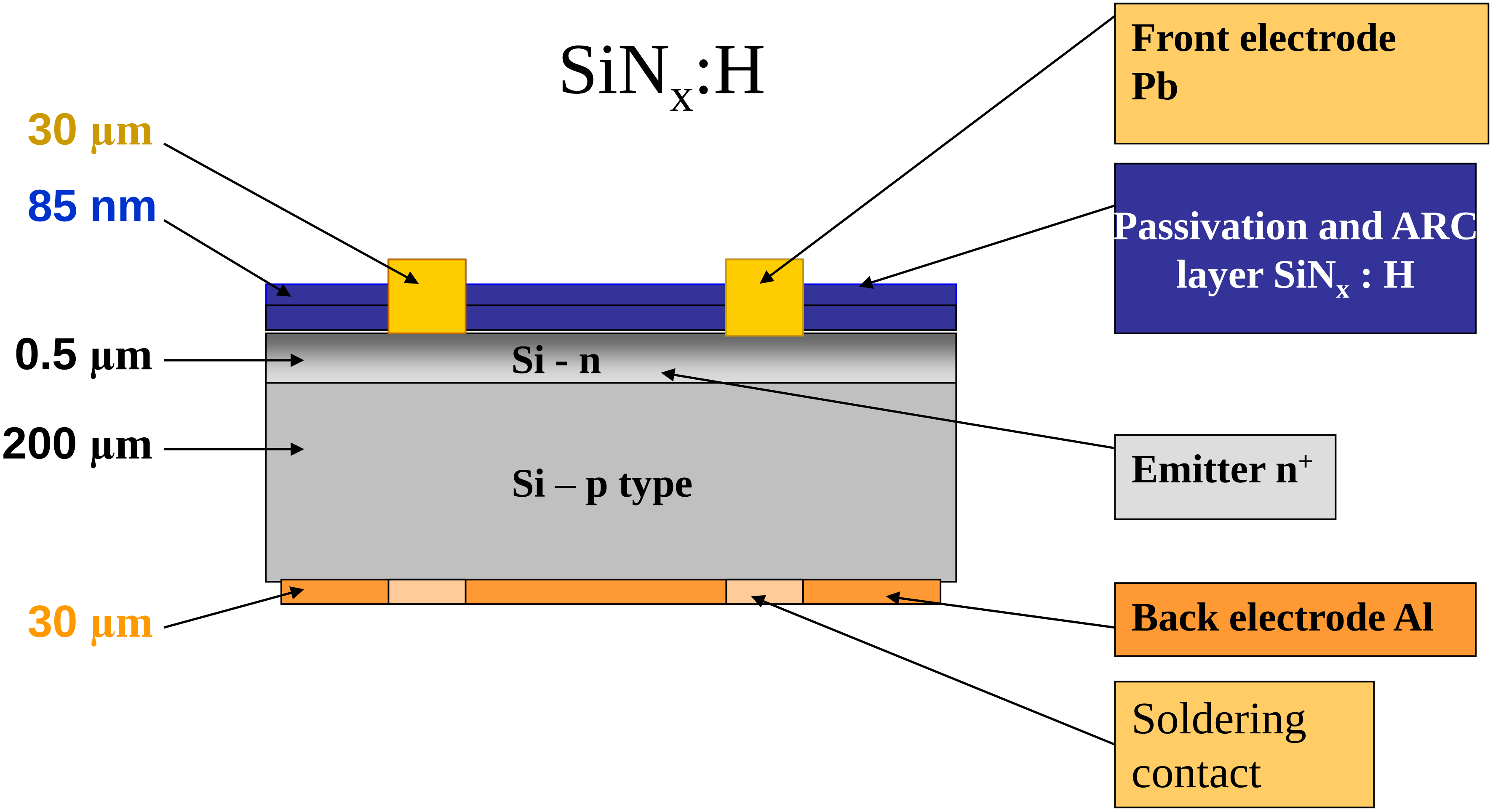
Scheme of solar cell section after metallization process



Al



Scheme of solar cell section after metallization with SiN_x:H as ARC layer

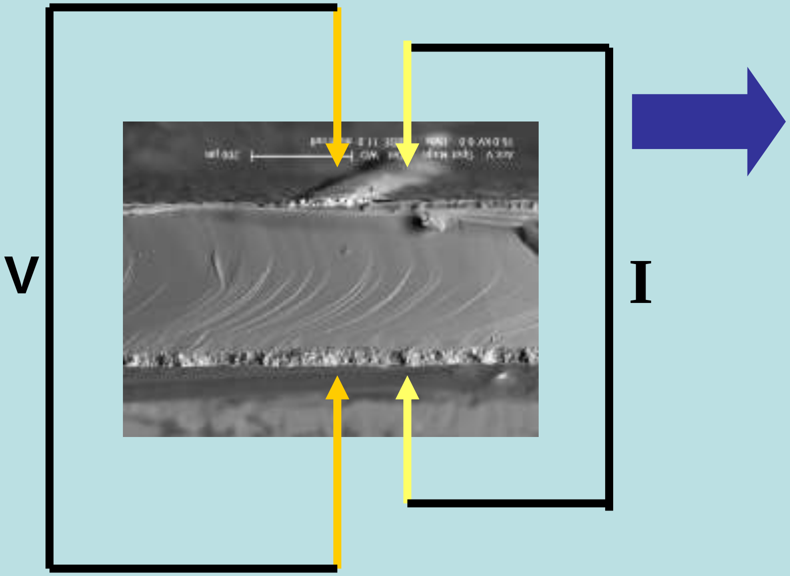


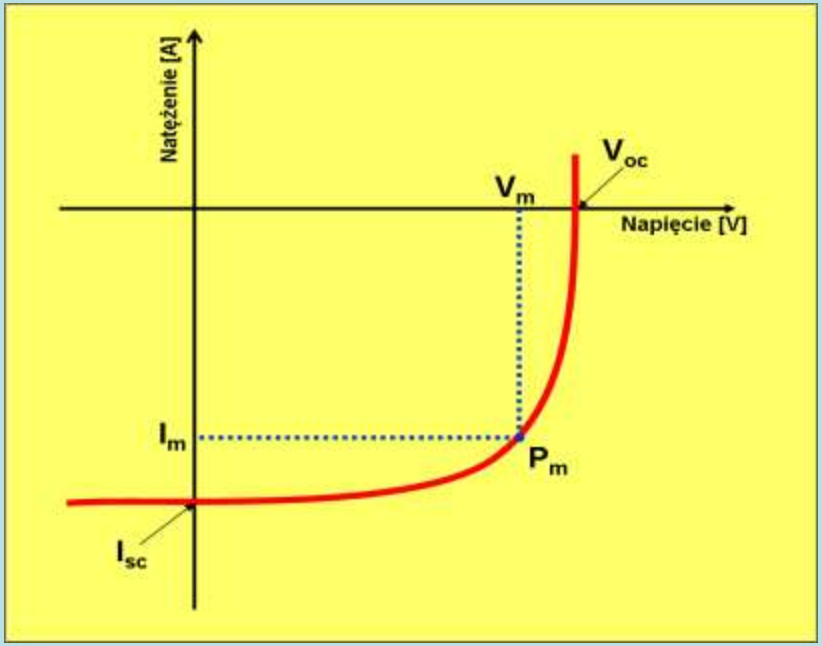
V Current-voltage characteristics measurements

One of the basic measurements of photovoltaic cells is the measurement of the light current-voltage characteristics (I-V). In the measuring system, one can distinguish three basic elements which determine the measurement quality, that is the light source, the measuring system, as well as the table and the contact probes. The I-V characteristics must be measured under strictly defined conditions for the given radiation spectrum and temperature, under so called STC (Standard Test Condition). The applied standard also includes the use of solar light simulators Class A, with the AM1.5 spectral matching tolerance within the rage of 0,75 ÷ 1,25 and with the acceptable inhomogeneity of the illumination intensity of ± 2 %, on the surface of the solar cell illuminated by the radiation with the intensity of 1000 W/m^2, and with the temperature of the cell equaling 25 ^{o}C

Solar simulator and I-V characteristic of a illuminated solar cell

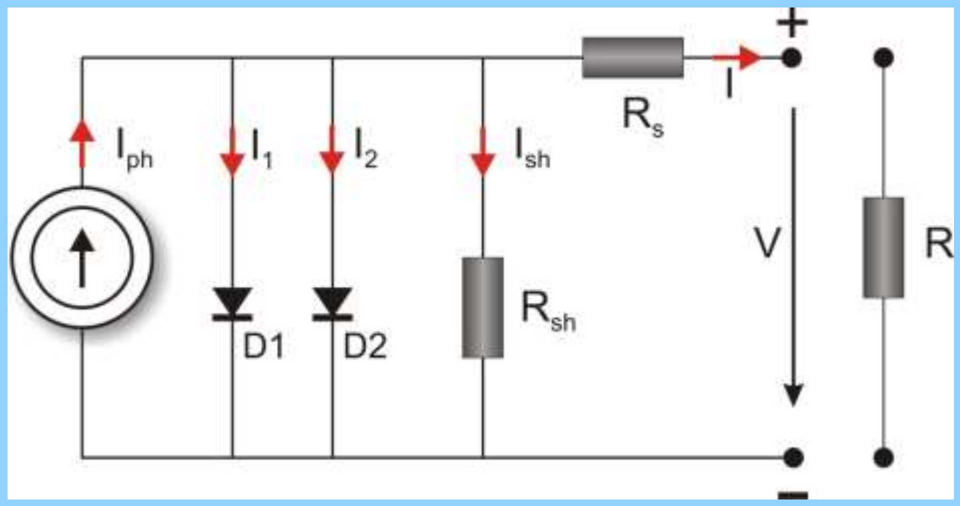
Electrical parameters of the solar cells





I-V characteristic

The numerical matching of the I-V characteristics with a single or double diode model makes it possible to calculate directly the value of the photocurrent, the voltage, the dark current, as well as the parallel and series resistance of the cell



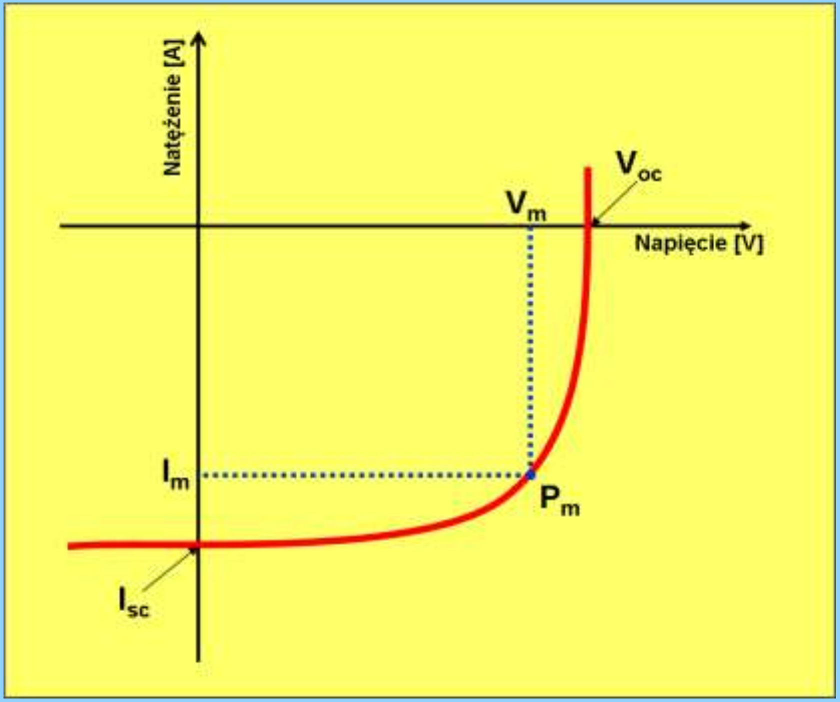
Scheme of the equivalent electrical circuit in a double diode model for an actual silicon solar cell

The mathematical model which describes the non-linear I-V characteristics of a solar cell is the equation with seven parameters, which one can obtain by applying Kirchhoff's Law to the equivalent circuit

$$I = I_{ph} - I_{S1}\left[\exp\left(\frac{q\left(V + IR_s\right)}{A_1 kT}\right) - 1\right] - I_{S2}\left[\exp\left(\frac{q\left(V + IR_s\right)}{A_2 kT}\right) - 1\right] - \left(\frac{V + IR_s}{R_{sh}}\right)$$

I_{S1} - saturation current of dark current diffusion component
I_{S2} - saturation current of dark current generation-recombination component
V - voltage possible to obtain from the solar cell
R_s - cell's series resistance
I_{sh} - leakage current
R_{sh} - cell's parallel resistance
A_1 - diode's quality coefficient (value close to 1)
A_2 - diode's quality coefficient (value close to 2)
R - external resistance

Knowing the above I-V characteristics, one can calculate the basic and most important values for the solar cell



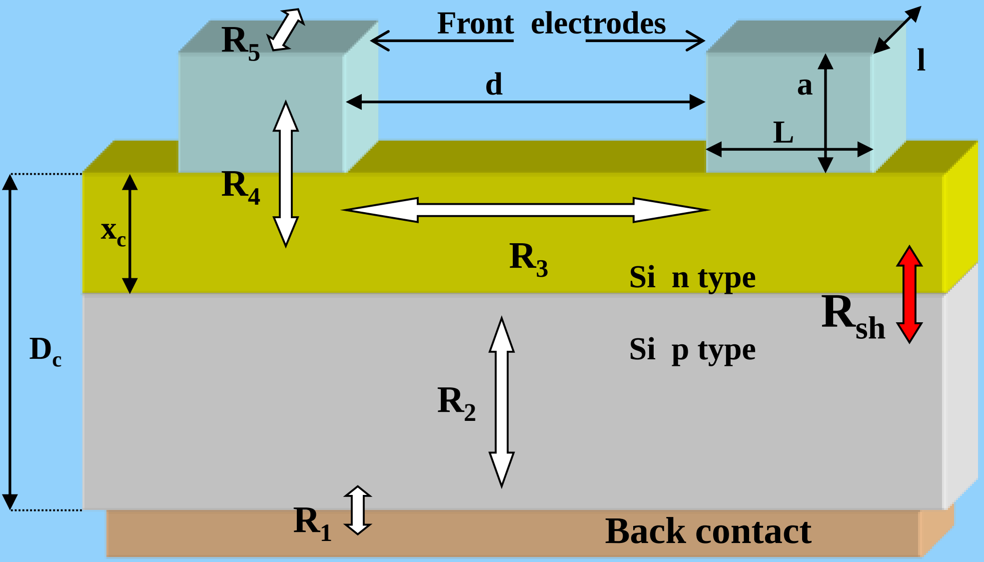
$$FF = \frac{I_m V_m}{I_{sc} V_{oc}} = \frac{P_m}{I_{sc} V_{oc}}$$

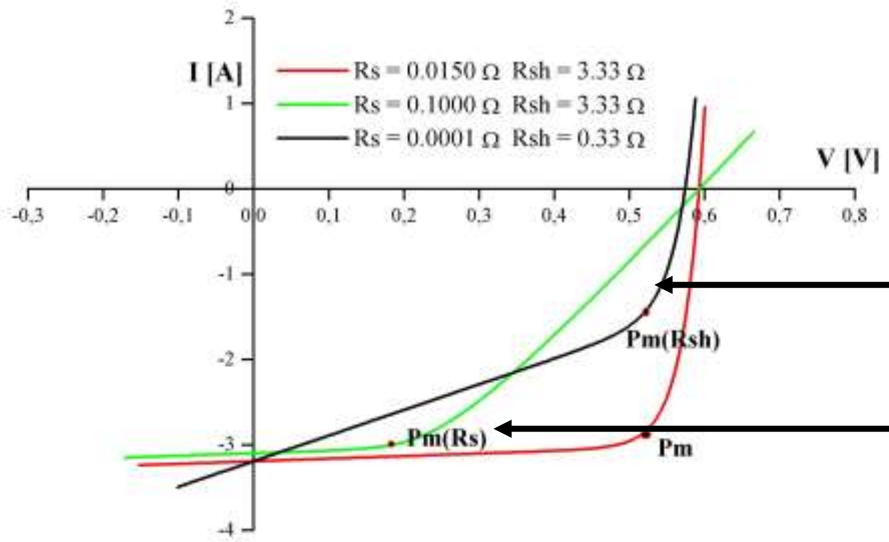
$$E_{ff} = FF \frac{I_{sc} V_{oc}}{P_{in} S} \cdot 100\%$$

Series R_s and shunt R_{sh} resistance influence on FF

$$R_s = \Sigma R_i$$

$$R_4 = \frac{\sqrt{R_\rho \rho_{con}}}{l} \coth\left(L \sqrt{\frac{R_\rho}{\rho_{con}}} \right)$$

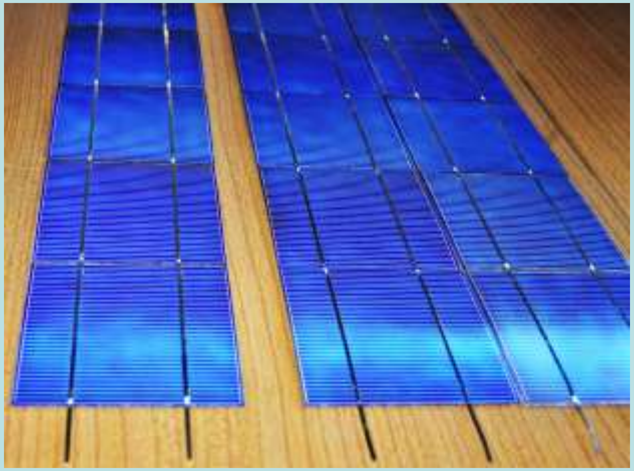




Small Rsh
(should have
Rsh >1 kOhmcm^2)

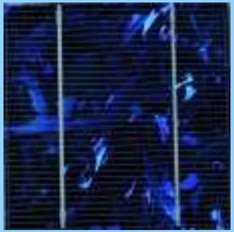
High Rs
(should have
Rs < 0.5 Ohmcm^2)

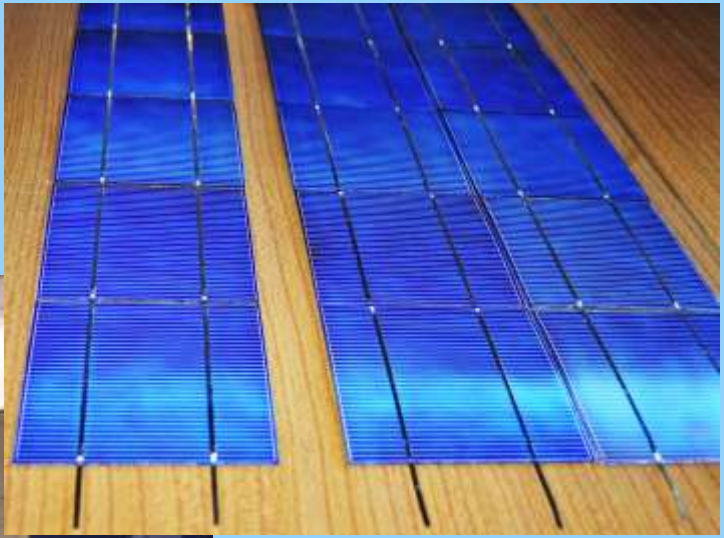
Solar cells are interconnected in a series to obtain a configuration that decides the required output current and voltage. To protect the cells from the environmental effects, the cells are fixed to a module in which the high transmission glass substrate type is the most commonly used design. PV modules carry a 25 year warranty. Solar encapsulates are typically made with ethylene vinyl acetate (EVA) and teflon backsheet foil. The completed laminate is than placed into the laminator machine, which is heated to a temperature of 150 ^{o}C for 15 min. to melt the encapsulant materials. During the lamination step, a membrane presses solar module made of glass, solar cells and foils with the pressure of up to 900 mbar. A vacuum is than applied to remove any air bubbles trapped during the process. While the glass provides the required durability and surface transparency, the backsheet provides physical protection, electrical insulation and a barrier to moisture ingress



Aiming at breakages equal to 0% with solar cells getting thinner and thinner, the was developed a new innovative soldering system by combining the traditional contact soldering, since always considered the highest quality of soldering with hot air. This special designed soldering system is optimized for the photovoltaic solar cells and permits to reach a very high quality soldering with more than 300 N in peel test. The ribbon is soldered on the entire cell serigraphy surface.

Stringer





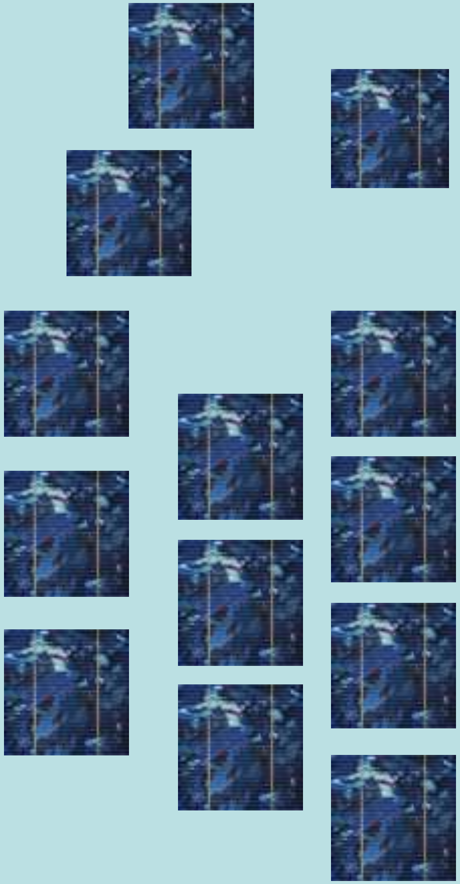
Technical Features of PV product

Electrolytic flat copper wire of high purity 99.95%, smooth, brilliant, cleaning. Out of scales and strokes, plated by dipping with tin and lead, or other lead-free chemicals compositions.

Composition of Plated Material:

Lead series products	Sn 60%, Pb 40%
	Sn 63%, Pb 37%
	Sn 62%, Pb 36%, Ag 2%
	Sn 60%, Pb 39.5%, Ag 0.5%
Lead-free series products	Sn 96.5%, Ag 3.5%(Bi)
	Sn 97%, Ag 3% and so on

Solar cells

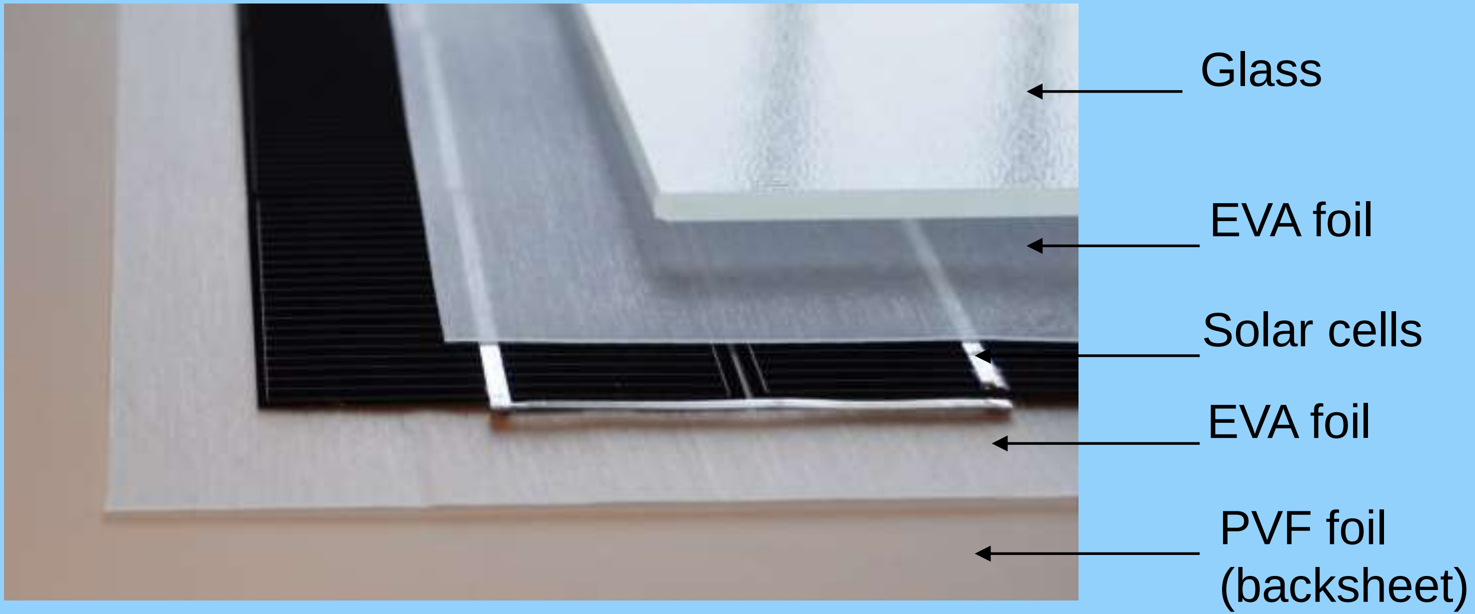


6 inches

36 (40) or 72 solar cells

PV module

Power 3 Wp – 250 Wp → 1000 Wp



EVA – ethylene-vinyl acetate
PVF – polyvinyl fluoride (tedlar)

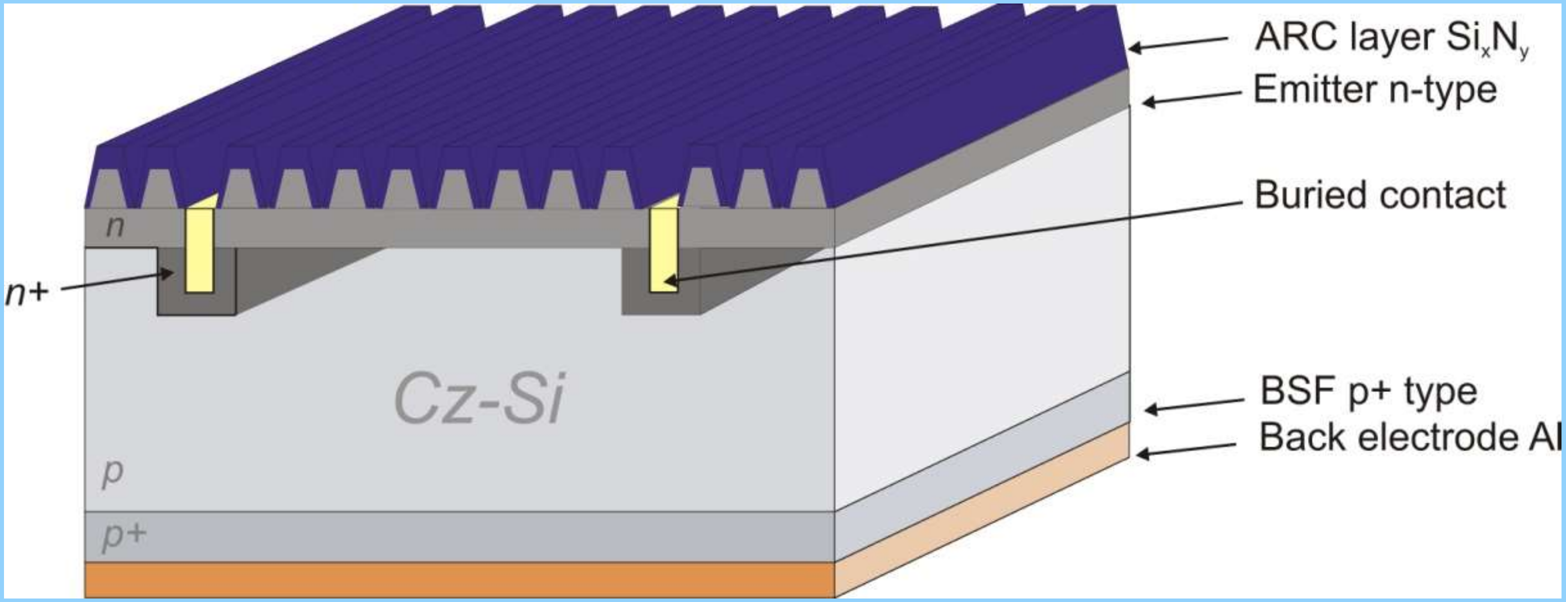
INSTITUTE OF METALLURGY AND MATERIALS SCIENCES

Industrial laminator L200 P.Energy

Directions of silicon solar cell development

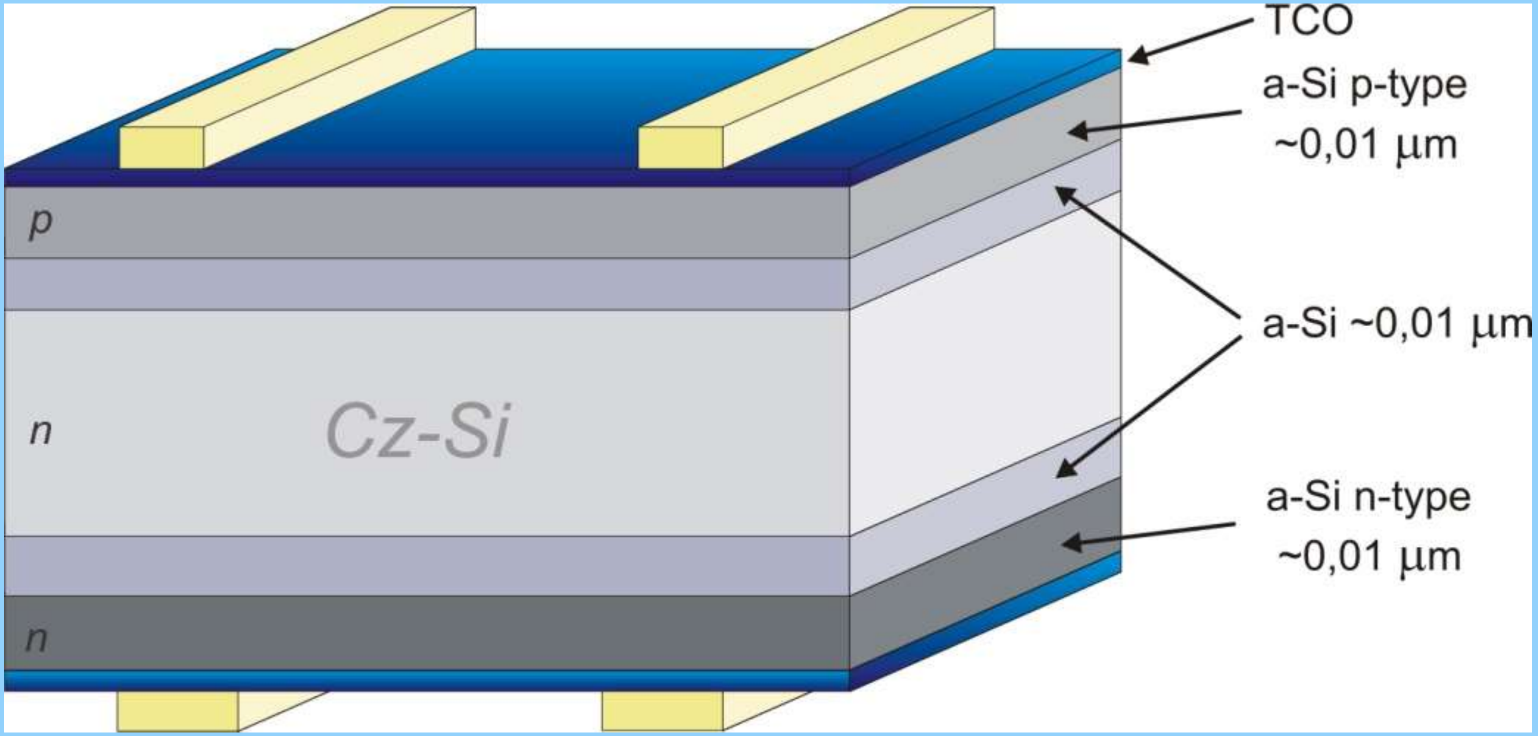
The basic trend in the research and development work is the reduction of the thickness of the solar cell’s base plate, from the currently applied 200 ÷ 150 μm down to 80 ÷ 120 μm, with a simultaneous reduction of the material lost in the process of cutting a single plate from a block, from the present 150 ÷ 120 μm down to 80 μm. This requires a full automatization of the production processes. This leaves a significant space for the concepts of solar cells allowing for a greater conversion efficiency Eff than that of the cells currently manufactured in the mass production, with the efficiency of 16 ÷ 19 %.

The highest conversion efficiency, 22 %, was obtained for a mono-crystalline BCSC cell, type FZ. The basis for achieving such a high efficiency is the application of the front electrode contacts made of a nickel-copper-silver layer, deposited by means of a chemical bath in the ~ 30 ÷ 50 μm deep laser-cut grooves. Applying a second donor diffusion through the mask makes it possible to create a strongly doped n+-type area under the contacts, with the laminar resistance at the level of 20 Ω/□, which affects the reduction of the series resistance. The high-resistant emitter Rρ ~ 120 ÷ 200 Ω/□, between the thin leading electrodes, reduces the disadvantageous effect of the Auger recombination process and allows for a significant improvement of the cell's current density.



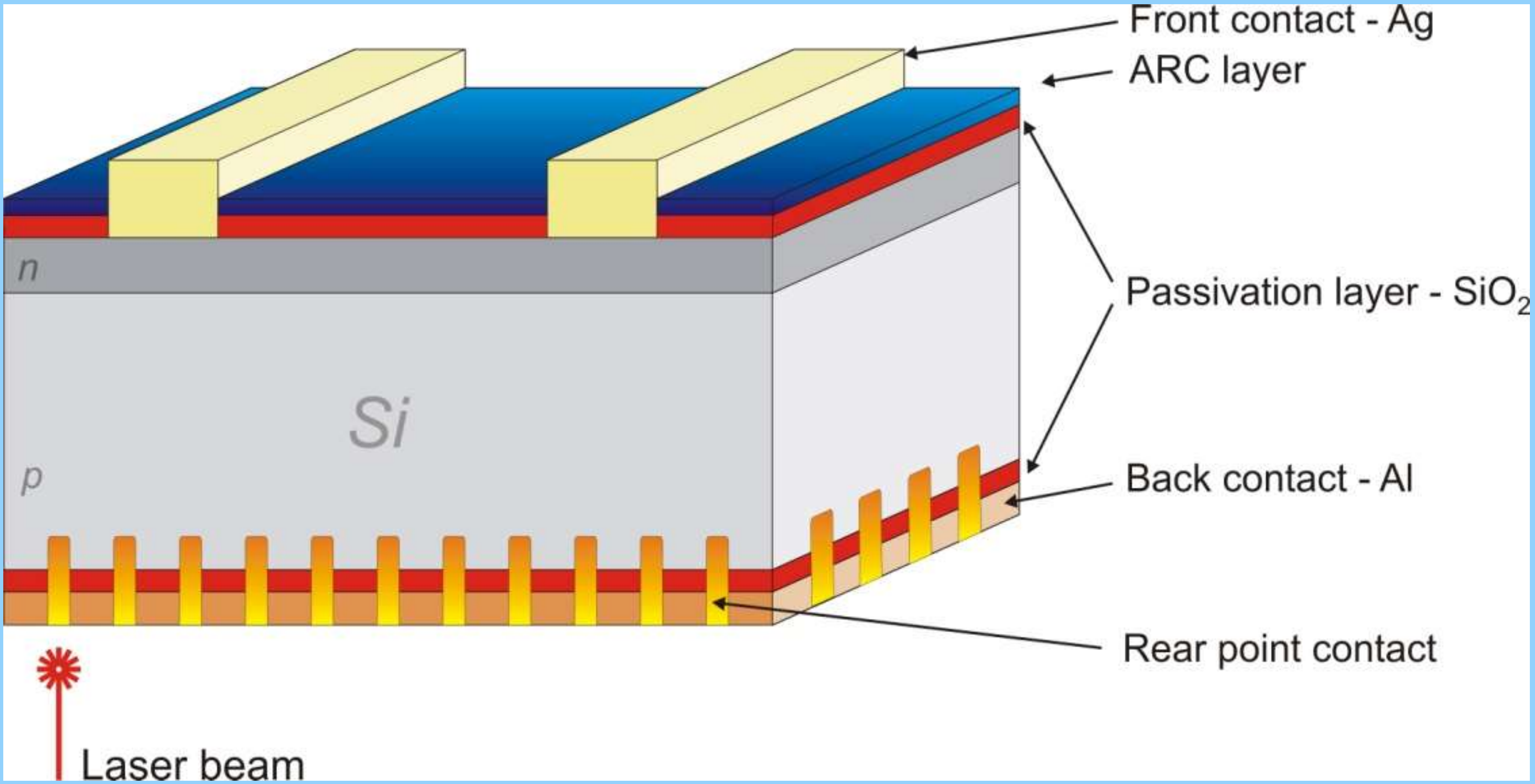
Cross-section of a mono-crystalline silicon solar cell with buried contacts (BCSC).

The efficiency of the HIT-type cells (*Heterojunction with Intrinsic Thin layer)* is the result of the excellent passivation of the silicon's surface, provided by the non-doped layer of hydrogenated amorphous silicon, which reduces SRV down to the level of 30 – 50 cm/s . What is more, the whole of the technological processes of the solar cell production is performed at the temperature below 200 °C, which does not cause the generation of additional recombination centers or silicon defects.



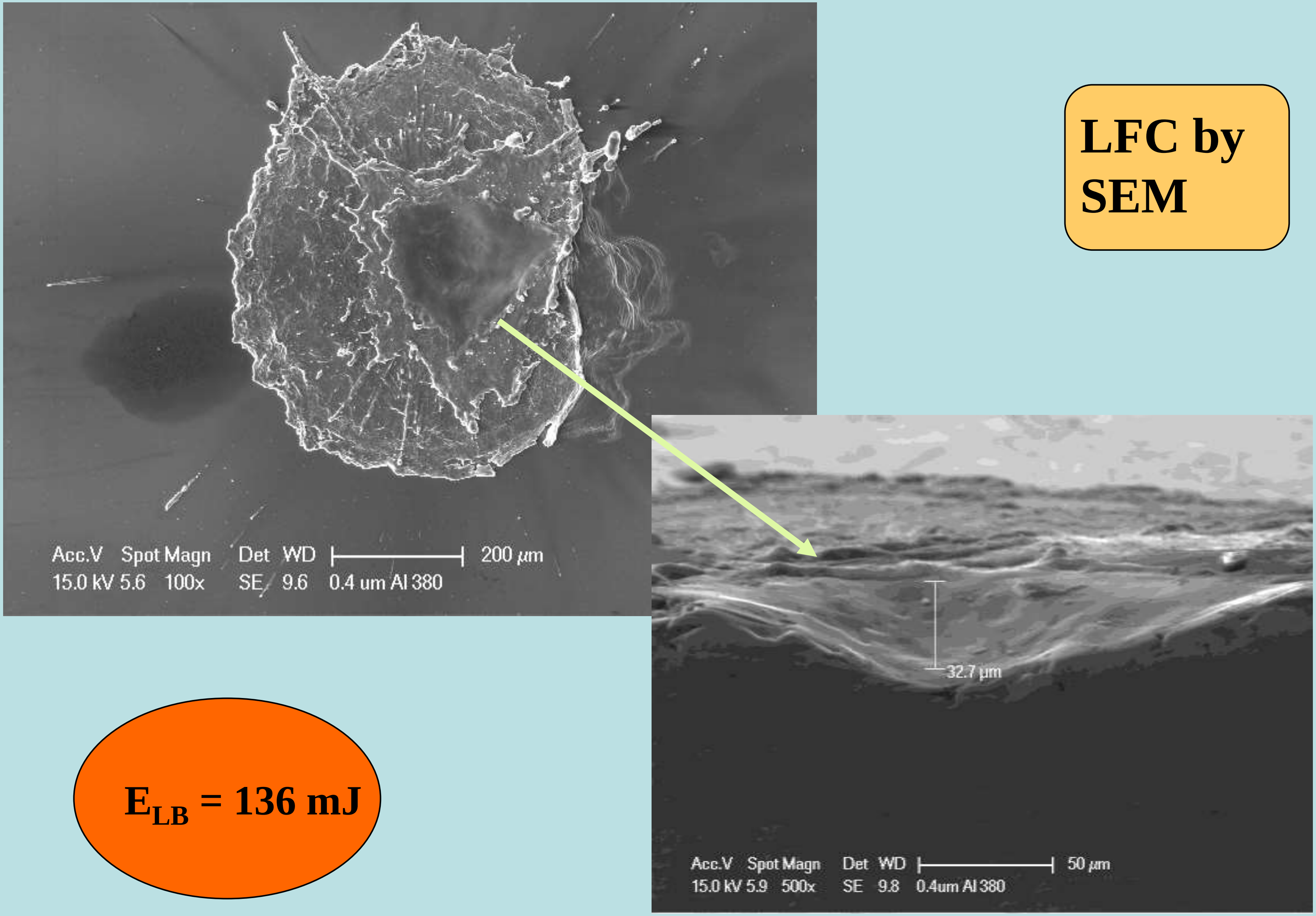
Cross-section of a mono-crystalline solar cell with double-sided layers of amorphous silicon (HIT)

The direction of research aiming at the achievement of the highest possible photovoltaic conversion coefficient with the minimum thickness of the crystalline plate, generates a significant problem resulting from the fact that the 30 µm-thin aluminium layer, used to obtain the rear contact, deposited with the screen printing method, causes the thin Si plates to bend and break, due to the difference in the thermal expansion coefficient, which equals $2{,}35 \times 10^{-6}$ K^{-1} for Si and $25{,}3 \times 10^{-6}$ K^{-1} for Al. What is more, the generated back Al layer has its reflection coefficient, within the longwave range, only at the level of 70 – 80 % and it allows for the SRV reduction on the back surface only down to the value of about 500 cm/s. Considering the above facts, one of the solutions is the passivation of the back surface of the cell and the creation of point contacts with the use of laser, which will allow to maintain a large fraction of the rear surface with the passivizing layer. This is implemented in the case of the LFC cells. A single contact point is a few hundred micrometers in diameter, and the distance between the consecutive points is within 1 mm.



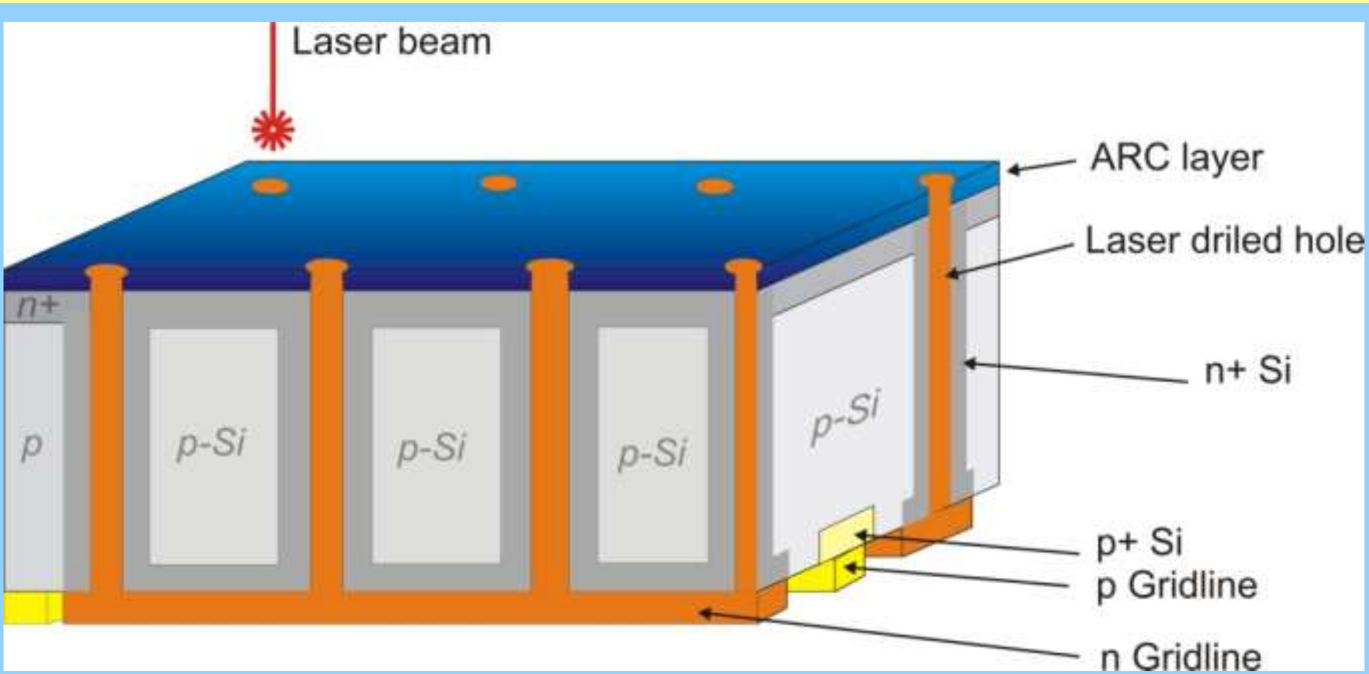
Cross-section of a solar cell with rear point contacts, produced with the laser LFC *(Laser Fired Contact)* method

LFC by SEM



E_{LB} = 136 mJ

Their most important distinguishing mark is the few hundred holes, ~ 100 μm in diameter, produced with the use of laser, whose wall-doping is the same donor type as that of the emitter, and this allows to localize the electrode contacts exclusively on the back side of the cell. This reduces the cover coefficient down to zero, which, in turn directly affects the increase of the short-circuit current's density Jsc of the cell. An additional advantage of the cells with the contacts localized only at their back side is the possibility of their assembly into a module without the sequential interweaving of the connection strips, which allows for a better packing of the cells and also creates the possibility of an integrated module assembly, that is soldering the cell layer with the previously prepared rear matrix of the module.



Cross-section of a solar cell with rear point contacts, produced with the laser LFC *(Laser Fired Contact)* method, and cells with an EWT *(Emitter Wrap Through)* emitter

Module EWT made by SOLLAND

Moduł EWT firmy SOLLAND

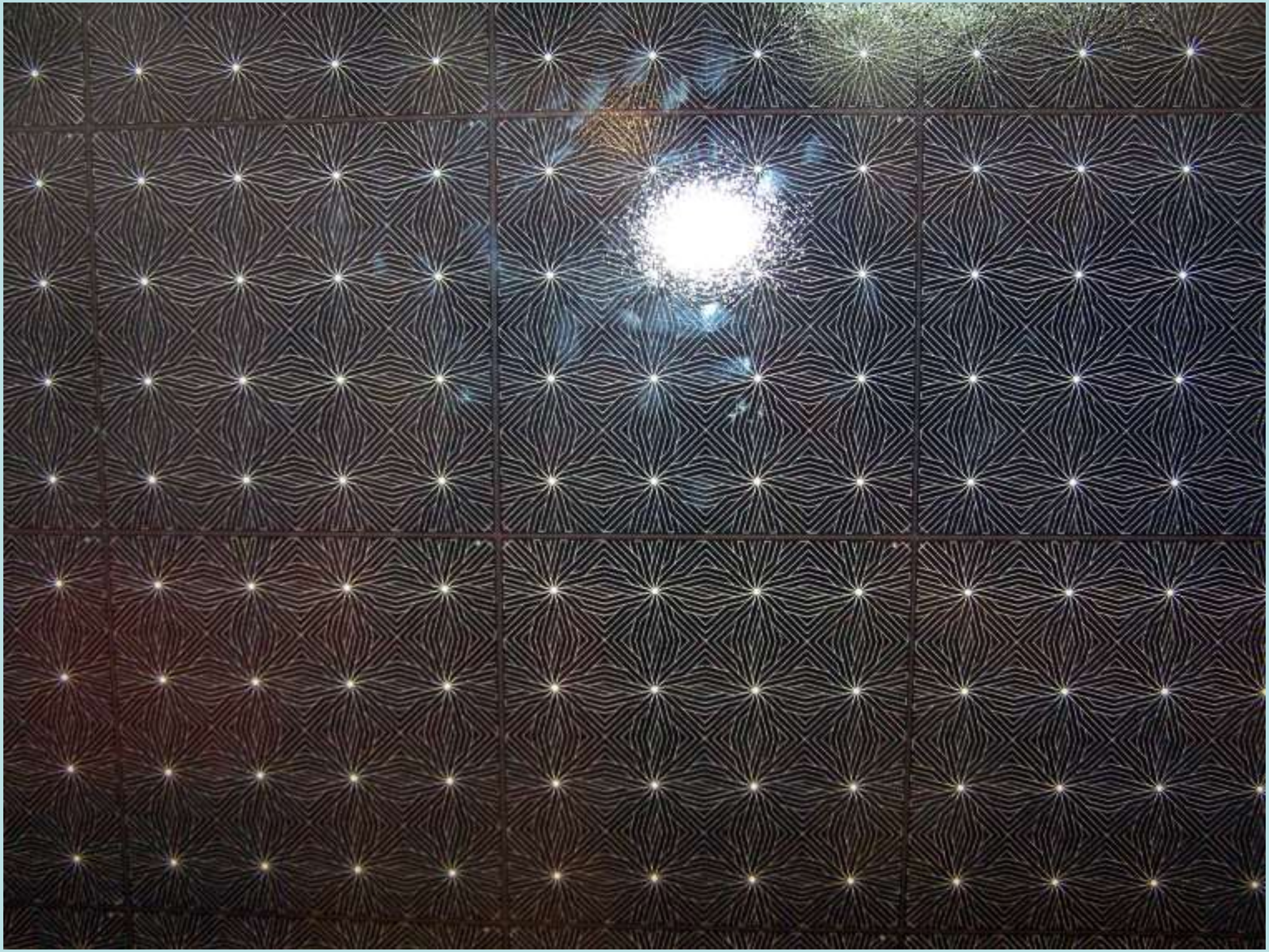
Sunweb®modules

60 cells
156 x 156 mm
Type MWT
Power 235 – 250 Wp
Temp. -40 °C ÷ +80 °C
Weight – 22 kg

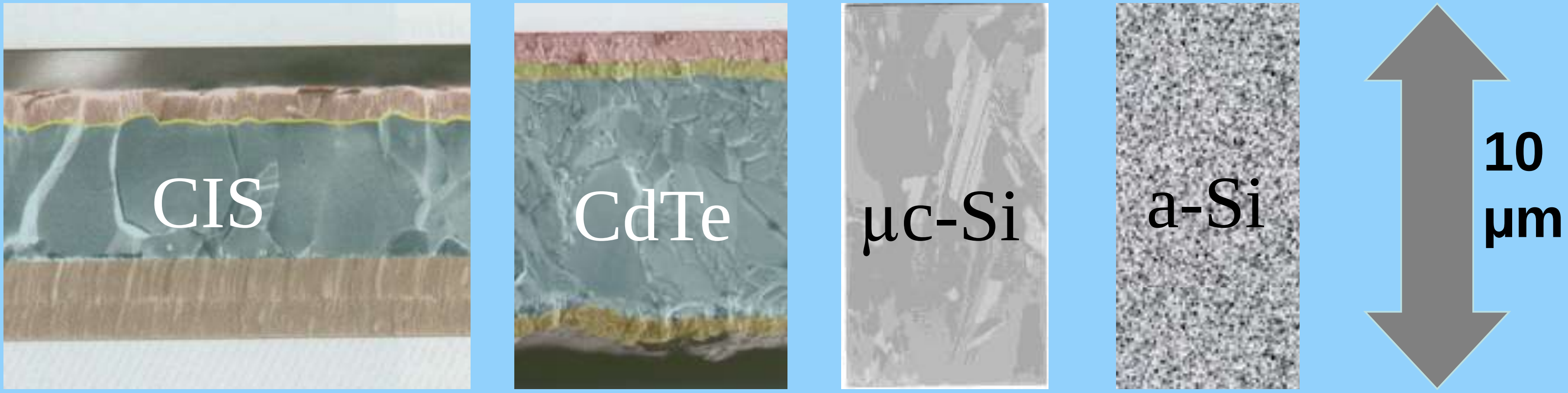
1,613 mm x 984 mm

Module EWT made by SOLLAND

16 holes performed LF



Thin film solar cells



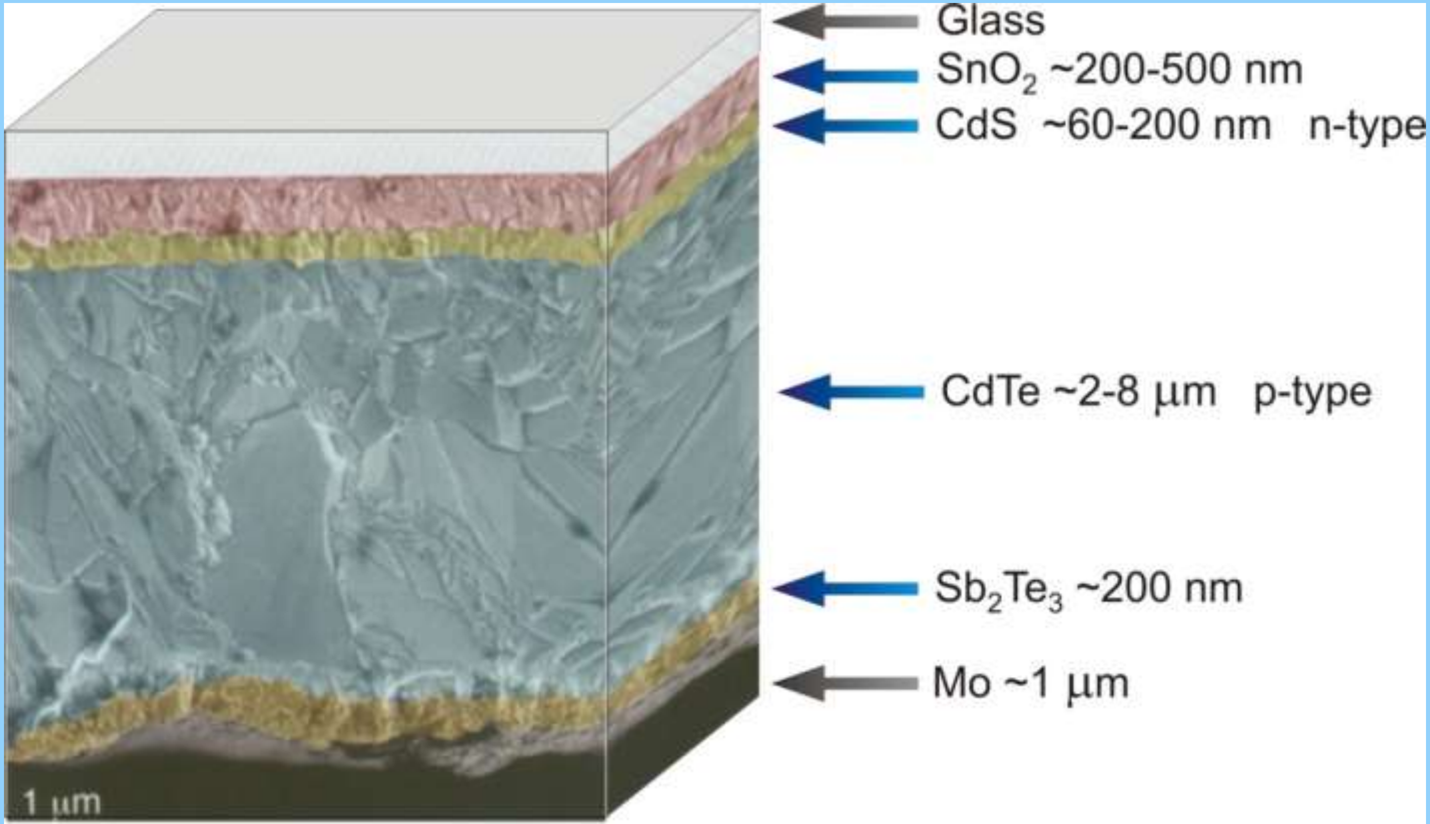
Thin film solar cells

Solar cells can be divided into two main groups: wafer based and thin films. The major drawbacks of wafer solar cells are that the Czochralski or casting process consumes a large amount of electrical power and when the wafers are cutting, there is a considerable wastage of crystal of about 33 %. Unlike crystalline silicon solar module manufacturing, in which the cells are constructed first and later interconnected, the creation of thin-film modules in the process in reverse. First, the absorber and conductive layers are deposited on the substrate and than separated so that they are monolithically connected in series. The interconnection is necessary to convert the high current and low voltage output into a low current and high voltage. This minimizes ohmic power losses, which scale as the square of the current. The most prominent thin film solar cells are: CdTe, CIS and a-Si/µc-Si or a-Si/mc-Si. Today thin film solar cells have a market share of about 12 %.

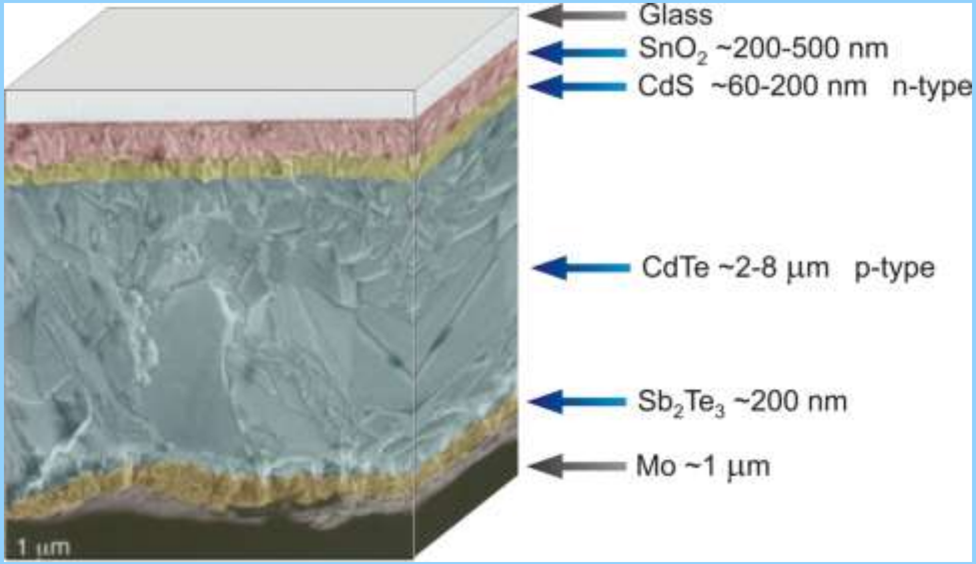
CdTe solar cell

Among the thin-layer solar cells, those of the greatest importance are currently the cells with a cadmium telluride base (CdTe), the latter having a simple energy gap Eg = 1,48 eV and a high value of the absorption coefficient $\alpha \sim 105\ \text{cm}^{-1}$, within the wavelength range of 300 ÷ 820 nm, which makes the layer, only a few micrometers thick, provide the absorption of almost all the radiation in the above range. The above cells are made with the method of depositing successive layers on a glass base covered with a thin layer of a transparent conductive oxide (TCO). The rear contact is achieved through a thin layer of metal. The significant advantage of such cells is the possibility to produce their successive construction layers by means of such techniques as a chemical bath, vapour deposition, electrolysis, magnetron sputtering, spraying or close space sublimation (CSS)

CdTe solar cell



Cross-section of a thin-layer CdTe cell with a typical kind of conductivity and thickness of particular layers



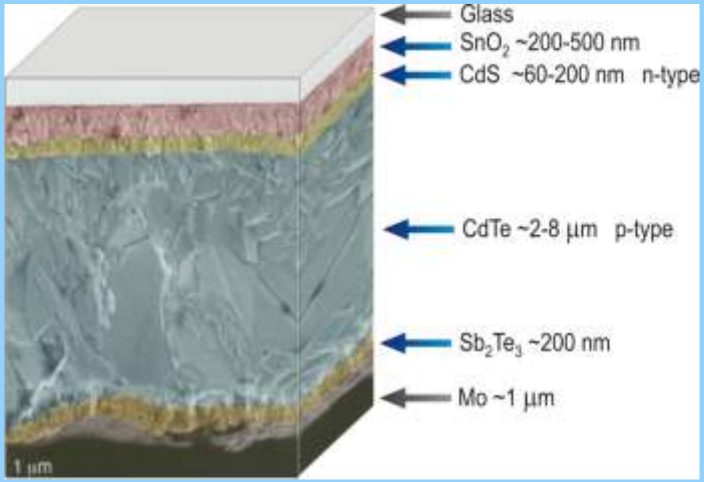
The SnO_2 layer, fluorine doped, is the transparent contact that provides current collection from the front side of the device. In thin film solar cells the TCO front contact needs a high transmission ~ 90 %, high bandgap ~ 3 eV, and high conductivity for use as a transparent contact in the top cell. The CdS layer serves as the window layer. The heart of the cell is CdTe layer, serves as the absorber for incident light. The Sb_2Te_3 layer produces an ohmic contact to the CdTe, and the Mo decreases the series resistivity of the back contact. The thickness of the CdS layer can strongly affect device performance. The cell with a CdS layer of 60 nm has lower open circuit voltage (Voc).

Thin Film Photovoltaic Transparent Conductive Oxide (TCO)

Overview: A transparent top contact is necessary to allow light into the solar cell layer stack. Most optically transparent and electrically conducting oxides (TCO) are binary or ternary compounds, containing one or two metallic elements. Their resistivity can be as low as 1×10^{-4} Ωcm, and their extinction coefficient in the visible range (VIS) can be lower than 0.0001.

The most prevalent TCO material systems are zinc oxide or indium oxide. Aluminum doped zinc oxide (ZnO:Al, AZO) or tin doped indium oxide (In_2O_3:Sn, ITO) are commonly used, however, other dopants and oxide combinations have been tested. Magnetron sputtering is an industrially proven, large area deposition technique that is typically used to deposit AZO or ITO. When considering a sputtering process, it is important to define your material system and also the type of deposition power.

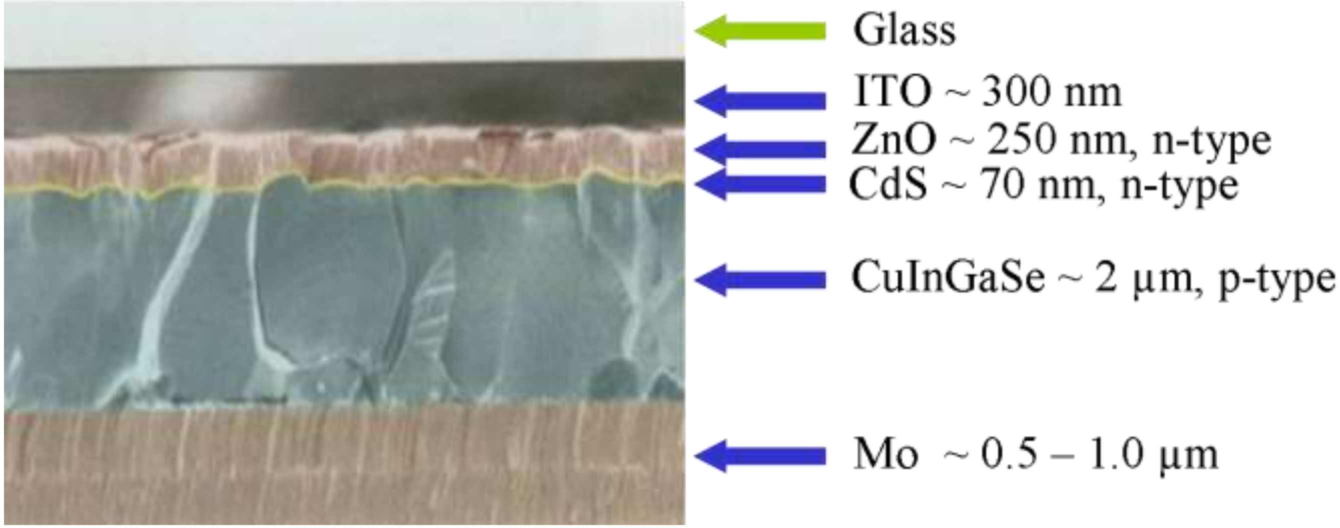
CdTe solar cell



Molybdenum is metal layer that is regularly used as a back contact layer for inorganic thin film solar cells, such as CIGS and CdTe. The most common method used to deposit Molybdenum is sputtering, especially in high volume manufacturing environments.

The advantages of a sputtered process include precise process control with scalable processes while still maintaining the ability to tune molybdenum layer properties for structure optimization. Reactive sputtering of molybdenum oxide has also been used as a buffer layer to improve the efficiency of thin film organic solar cells

CIGS solar cell



The basic schematic cross sectional view of CIGS thin film solar cell

The CIGS layer stack is most commonly deposited on Soda Lime Glass (SLG); however, many companies are also looking at lighter, more flexible substrates such as polyimide or metal foils.

CIGS solar cell

- Technology process

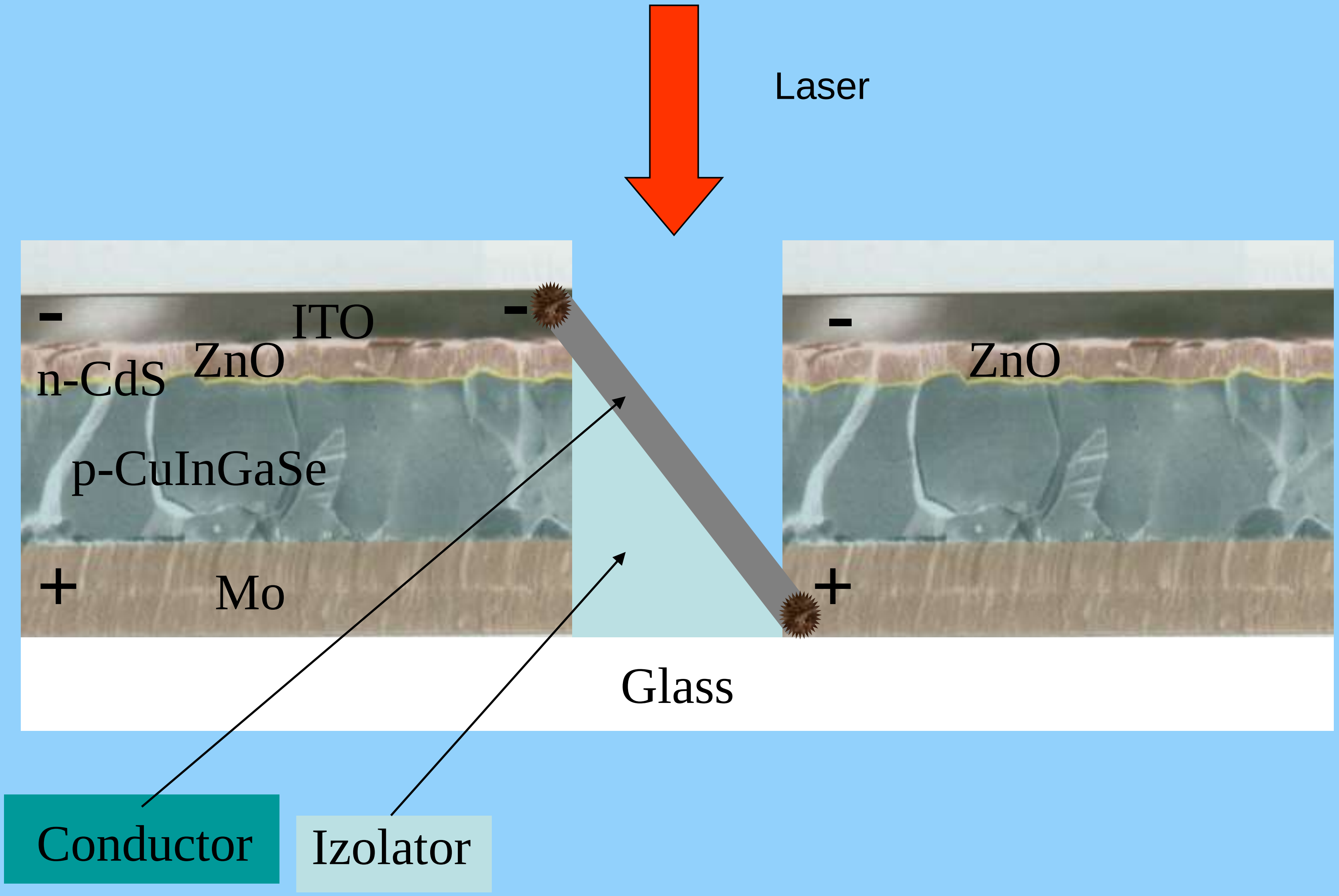
Step 1: Glass preparation
Step 2: Sputter deposition of molybdenum
Step 3: Patterning of the molybdenum conductor
Step 4: Compound formation to create CIGS
Step 5: Patterning to open up the CIGS material
Step 6: Sputter deposition of the zinc oxide transparent conductor
Step 7: Patterning of the zinc oxide
Step 8: Encapsulation
Step 9: PV module testing

CIS ($CuInSe_2$) is a one of the most light absorbent semiconductor and only 0.5 μm can absorb 90 % of the solar spectrum but on the other hand it is very complex material what makes it difficult to manufacture. Its bandgap of 1 eV is rather low and it is usually replaced by an alloy of indium and galium and it is found as CIGS ($Cu(In,Ga)Se_2$) cells. Its bandgap can be varied continuously between 1,0 – 1,68 eV, depending on the Ga/InGa ratio. Many applications require high specific power and CIGS cells on light weight and flexible substrates can yield more than 1,5 kW/kg specific power. The industrial methods for CIGS synthesis employ: DC magnetron sputtering, Nd:YAG laser pattering, vacuum deposition and chemical bath deposition. The Indium is also used in flat screens, light emitting diodes and touchscreens and its exploited resources know today are approximately 11 000 tons what has a negative effect on the future ability of the CIGS technology. Long life CIGS modules have only been possible when encased between glass. This is because the front contact made of zinc oxide is very susceptible to humidity. The main producer of CIGS modules is Wurth Solar (Germany).

CIGS solar cell

- Technology process

The Mo layer is deposited on the glass by DC magnetron sputtering. This process is carried out in a multi-chamber, in-line sputtering system, where properties of the Mo are sensitive to the sputtering conditions. After laser patterning of the Mo, the glass substrate is transferred to another in-line vacuum system where extensive use is made of sources capable of downward evaporation. Three custom designed sources are employed to supply the Cu, In, Ga and Se needed to form the $Cu(In,Ga)Se_2$ compound. During this process the glass is heated. After deposition of the CdS and scribing of the CIGS, a second in-line sputtering system is used to deposit highly conducting zinc oxide as the top transparent electrode. This electrode is then patterned by scribing, and the plate is ready for testing.



Laser

\- ITO

\-

\-

ZnO

n-CdS

ZnO

p-CuInGaSe

\+

Mo

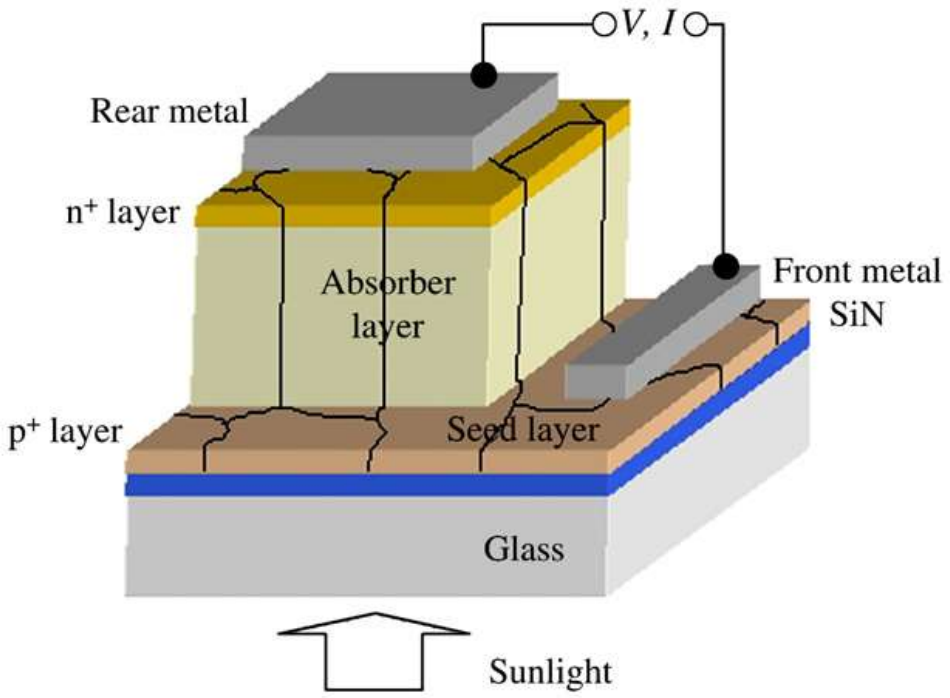
\+

Glass

Conductor

Izolator

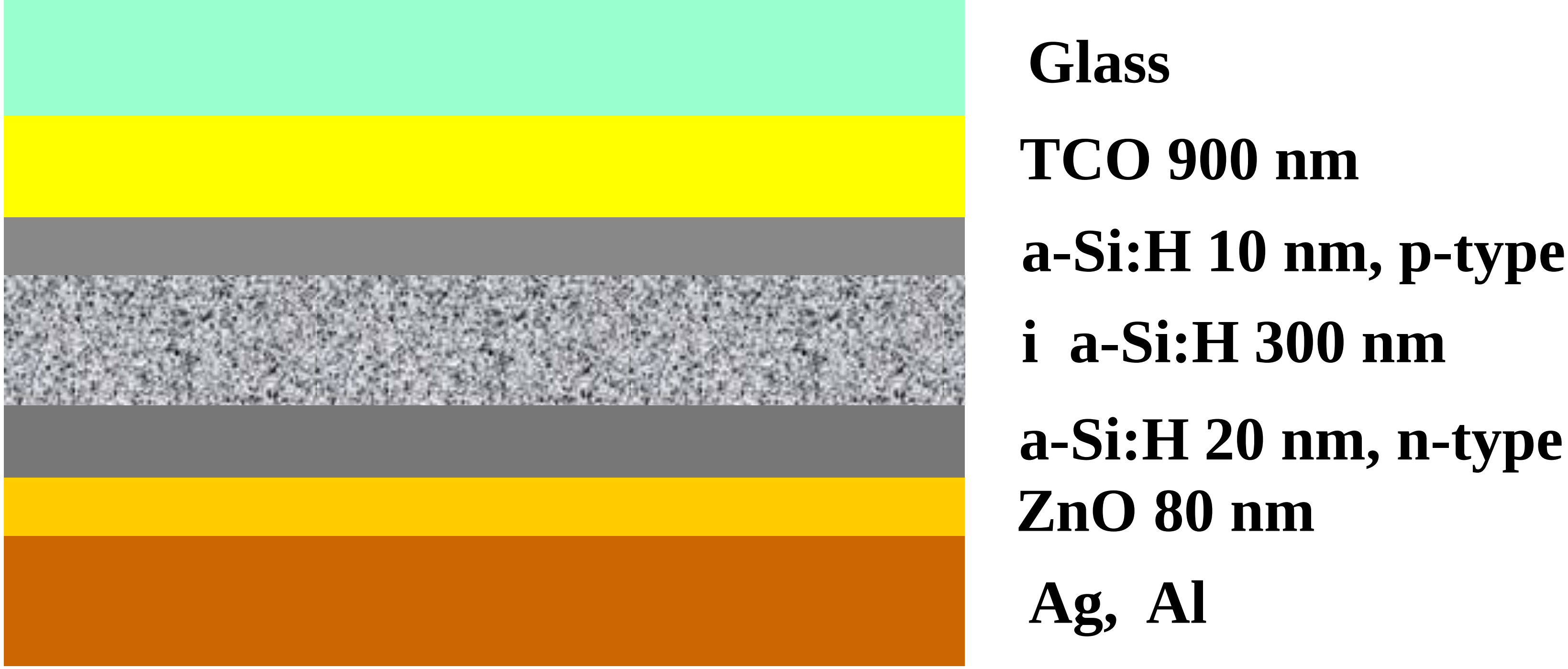
Schematic of a Mesa-type ALICIA poly-Si thin-film solar cell on glass
The sunlight enters the solar cell through the glass



The device is known as the ALICIA solar cell (ALuminium Induced Crystallisation, Ion Assisted deposition), A thin polycrystalline Si seed layer is made on a silicon nitride coated glass substrate by aluminium-induced crystallisation.
This seed layer is about 200 nm thick, has an average grain size of about 20 μm, and is heavily p+ doped with aluminium. Using this thin layer as a crystal template, an n-type layer about 1.8 μm thick is epitaxially grown on top, thus forming the p-n junction and the absorber layer of the solar cell. A heavily n+ doped layer is finally grown as a back surface field and contact region.

a-Si:H

Eg = 1.7 – 1.8 eV



Glass

TCO 900 nm

a-Si:H 10 nm, p-type

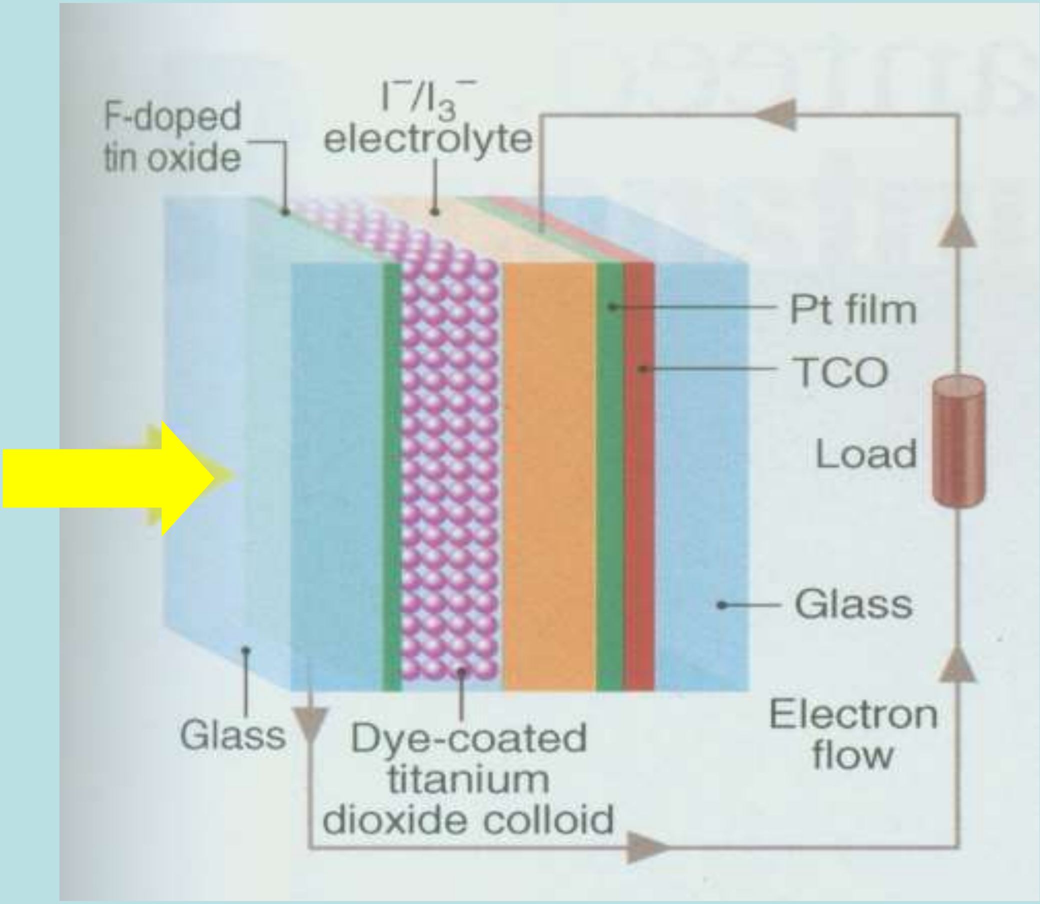
i a-Si:H 300 nm

a-Si:H 20 nm, n-type

ZnO 80 nm

Ag, Al

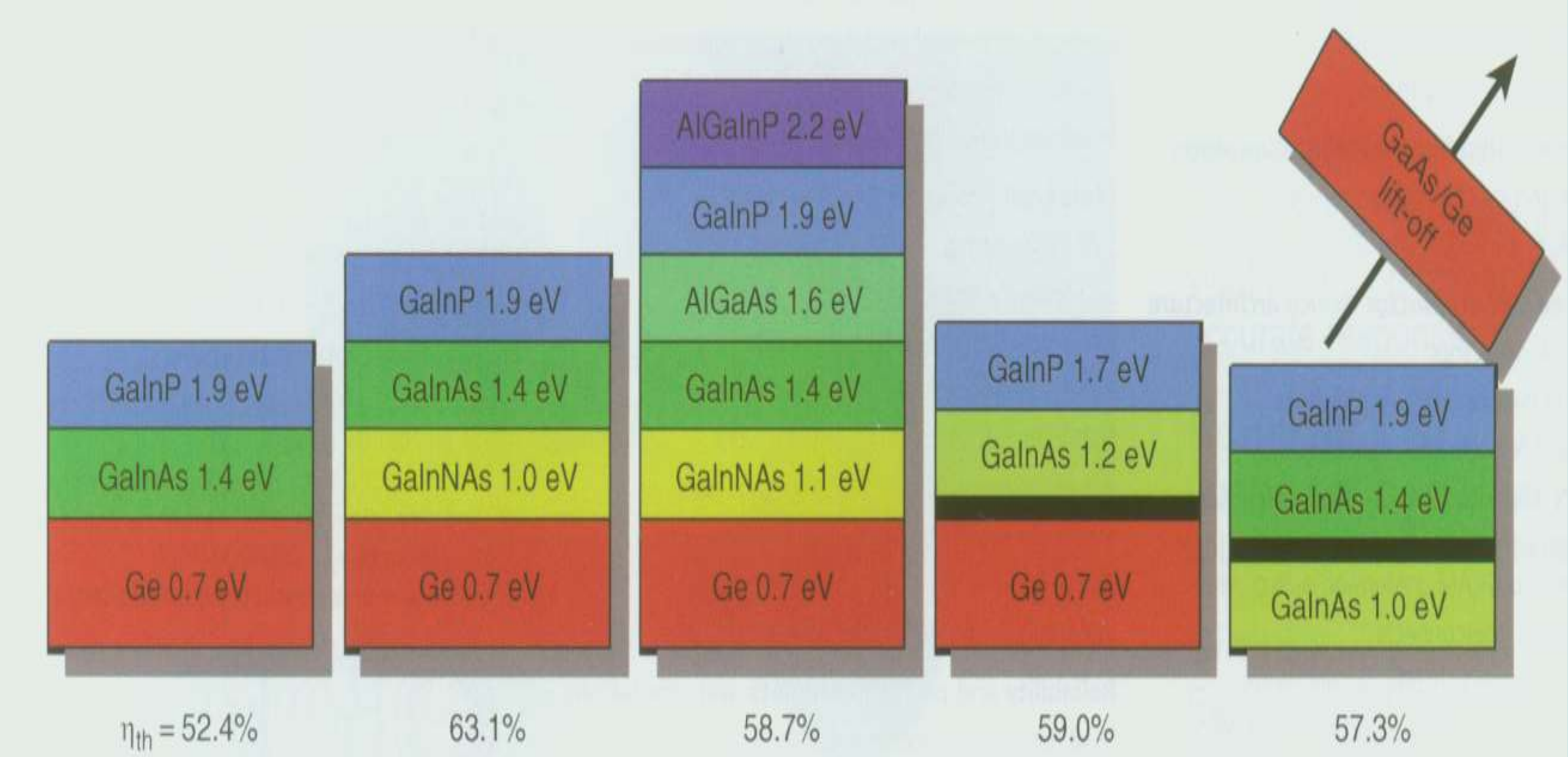
(Grätzel cell)



MRS Bulletin, 32, 2007

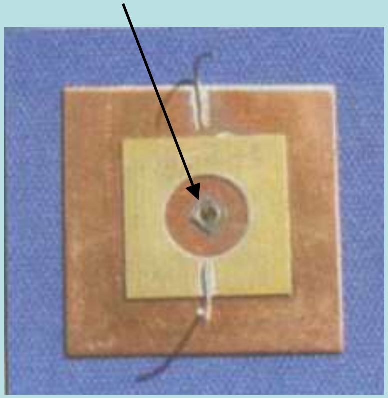
High efficiency Multijunction solar cells

For example: $E_g = 0.7 – 3.4$ eV for $In_{1-X}Ga_XN$



Concentrators

Solar cells
5 mm^2



Sun concentrator - 50 cm^2

At the solar
cell surface
the

„1000 Sun"

is focused