# CRYSATLLINE SILICON SOLAR CELLS IN MANUFACUTRING TECHNOLOGY ASPECTS – THE CHEMICAL PREPARATION AND JUNCTION FORMATION.

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**ABSTRACT**

In this paper, the second part of the technological process of manufacturing crystalline silicon solar cells realised in the Photovoltaic Laboratory of Institute of Metallurgy and Materials Sciences of the Polish Academy of Sciences (PL IMMS PAS) - Photovoltaic Laboratory at Kozy is presented. The described process is based on diffusion from $POCl_3$ resulting in emitter with a sheet resistance on a level 60 ohm/square. Some aspects playing a role in junction preparation process are discussed. Summarising, this paper gives also o brief overview on the chemical preparation and junction formation process made in the Photovoltaic Laboratory of PAS.

keywords: solar cell, crystalline solar cells, solar cells technology

## Chemical preparation of the wafers

During the process of cutting silicon ingots into wafers, saw damage is produced on the surface of silicon crystals. This saw damage induces defects of the silicon. For this reason, after first rinsing in acetone, all samples were etched in KOH (30%) to remove saw demage material 7 to 8 μm thick from each side of wafers. It is necessary for the preparing "as cut" silicon wafers delivered from manufacturer. As a result of wafer cutting from silicon ingot approximatly to 7 μm material from both sides of wafer is highly defected and must be removed. The next step is texturization in IPA:KOH (40%):DI$H_2O$ in volume ratio 3:1:46 solution at 80 $^oC$ for 15 min. and after that rinsed in HCl (2%) and HF (10%). All the chemical processes were completed by rinsing in deionized water and drying in $N_2$. The acide etching beeing isotropic method is still under our investigation [1,2]. Figure 1 shows the texturized surface of monocrystalline silicon wafers ethced in IMIM PAS Laboratory.

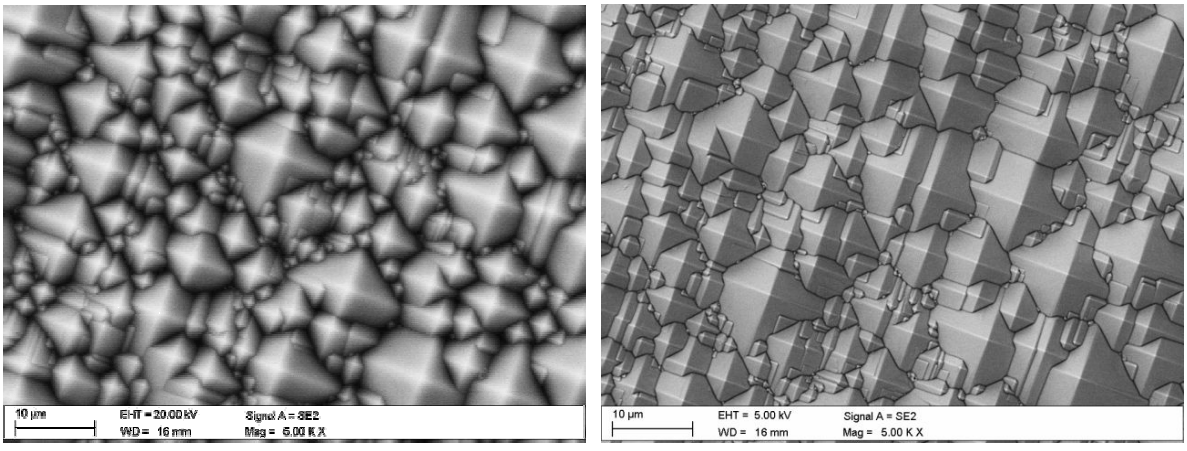


Fig. 1. Texturized surface of monocrystalline silicon (SEM)

The wafers were chemically etched and cleaned and the precise chemical procedure aims cleanning wafers before diffusion process is presented in table 1.

**Table 1.** Chemical processing applied to "as-cut" silicon wafers.

| **Chemical process** | **Chemical recipe** | **Time [min.]** | **Temperature [$^{o}$C]** |
|---|---|---|---|
| Organic contamination removing | Acetone | 10 | 25 |
| Rinsing | Deioznized water (DI $H_2O$) | 10 | 25 |
| Usuwanie warstwy zdefektowanej | 20% KOH | 3-4 | 80 |
| Rinsing | DI $H_2O$ | 10 | 25 |
| Surface texturisation | Isopropanol IPA+$H_2O$+ KOH | 30 | 80 |
| Rinsing | DI $H_2O$ | 10 | 25 |
| Neutralisation of potassium traces | $H_2SO_4$ 98%+ DI $H_2O$ 1:1 | 10 | 25 |
| Rinsing | DI $H_2O$ | 10 | 25 |
| Metallic contamination removing | HCl 2% | 10 | 25 |
| Rinsing | DI $H_2O$ | 10 | 25 |
| Native oxide removing | HF 5% | 2 | 25 |
| Rinsing | DI $H_2O$ | | |
| Drying | - | 1 | 25 |

Moreover, the Photovoltaic Laboratory of IMIM PAS carry on research on multicrystalline silicon wafers texturizarion using acid solution. In this case saw damage etching and texturization is carry on the same process. Advantage of this method in comparison with KOH etching is better surface homogeneity without faults on grain boundaries and least lover reflection coefficient. The chemical procedure aims acid etching multicrystalline wafers before diffusion process is presented in table 2.

**Table 2. Acid etching applied to ''as-cut'' multicrystalline silicon wafers.**

| **Chemical process** | **Chemical recipe** | **Time [s]** | **Temperature [°C]** |
|---|---|---|---|
| Rinsing 1 | DI $H_2O$ | 300 | 25 |
| Etching | HF+$HNO_3$+$H_2O$ | 60 | 25 |
| Rinsing 2 | DI $H_2O$ | 240 | 25 |

## The emiter formation

For both mono- and multicrystalline Si, a semiconductor homojunction was formed by diffusing phosphorus (an n-type dopant) into the top surface of the boron doped (p-type) Si wafer. Before diffusion processes the native oxide on silicon wafers was removed by diluted HF. Emitter diffusion is one of the crucial steps in the manufacturing process of silicon solar cells. To realize high efficiency, the quality of emitter is critical. One of the steady trend in the manufacture of the silicon solar cells is to produce the cells based on the higher and higher size area wafers. It is connected with financial possibilities and new equipment especially new diffusion furnaces.

There are this two methods of emitter of solar cell manufacturing in the Laboratory of IMMS PAS.

The emitter can be formed either by batch deposition of $POCl_3$ gas or spray deposition of liquid phosphoric dopant. The process has been optimized over the years to give reproducible performance. The emitter was generated at temperature 840 °C for 25 min. in an open quartz tube using liquid $POCl_3$ as the doping source. The parameters for the diffusion process in open quarzt tube furnace are described in table 3. This results is an emitter with a ssheet ressistance around 50 Ohm/sq.

**Table 3.** The parameters for the diffusion process in the open quartz tube furnace

| **Process** | **$N_2$ [l/min]** | **$O_2$ [$cm^3$/min]** | **$POCl_3$ [mg/min]** | **Time [min]** | **Temperature [°C]** |
|---|---|---|---|---|---|
| drawn in | 0,5 | 0 | 0 | - | - |
| stage 1 | 1 | 100 | 0 | 10 | - |
| stage 2 | 2 | 200 | 70 | 20 | 840 |
| stage 3 | 1 | 0 | 0 | 5 | - |
| exit | 1 | 0 | 0 | - | - |

The second method of emitter layer formation used in IMIM PAS Laboratory is diffusion process in IR (Infra Red) belt furnace using as dopant source liquid phospforous glass made by Filmtronics corporation. A conveyor belt IR furnace with fitted tungsten filament lamps, heating top and bottom of the belt was used for emitter diffusion process. The three following heating zones are 180 mm, 360 mm and 180 mm long and the belt speed was 15, 20 and 25 cm/min. In the IR furnace, silicon wafers are heated partly by direct IR radiation, partly by the contact with the hot conveyor belt and with the hot gasses within the furnace chamber [3]. The parameters of the diffusion process are given in Table 4.

**Table 4.** The parameters for the diffusion process in the IR furnace

| Process No. | Belt speed [cm/min] | Temperature [°C] Z1, Z2, Z3 | | | Time [s] | Sheet resistance RS [Ω/□] | Standard deviation Sd | Silicon type |
|---|---|---|---|---|---|---|---|---|
| 13-multi | 25 | 920 | 920 | 920 | 182 (~3 min) | 45 | 3.5 | multi-Si |
| 14-multi | 25 | 930 | 930 | 930 | 182 (~3 min) | 37 | 2.2 | multi-Si |
| 15-multi | 25 | 940 | 940 | 940 | 182 (~3 min) | 30 | 1.2 | multi-Si |
| 20-mono | 15 | 920 | 920 | 920 | 304 (~5 min) | 37 | 2.5 | mono-Si |
| 19-mono | 20 | 920 | 920 | 920 | 228 (~3.8 min) | 39 | 1.9 | mono-Si |
| 21-mono | 25 | 920 | 920 | 920 | 182 (~3 min) | 46 | 3.1 | mono-Si |

This process is based on Filtronics P509 dopant source and resulting in emitter with a sheet resistance on a level 45 ohm/square and p-n junction depth is around 0.3 μm.

The sheet resistance mapping tool is every time using to optimize the emitter uniformity (which is critical to contact formation), junction depth and phosphorus surface concentration to characterize the inline emitters.

Fig. 2. The industrial furnace for diffusion and heat treatment processes (PIE) and infrared belt furnaces (RTC type LA-310).

## Parasitic junction removal

After diffusion the wafers are covered by phosphorus-silicate glass PSG and have a donor doping layer on both sides and edges. At first diffusion the parasitic junction has was removed by means a special Teflon clamp in which the wafers were immersed in HNO3(65%):HF(40%):CH3COOH(80%) solution in the volume ratio 5:3:3 for 1 min. Then the PSG was removed in a 10 % HF solution for 2 minutes and the wafers were dried in a spin-drier in an atmosphere of highly purified air.

## Passivation process

In order to obtain high efficiency it is necessary to reduce the surface recombination losses. The standard technique for the reduction of the surface state density of Si is thermal oxidation. Surface passivation was achieved by the growth of thin, invisible passivating oxide $SiO_2$ at temperature 800 $^oC$ for 15 min. in $O_2$ and $N_2$ ambient atmosfere.
As stated above this process is not necessary in the case if SiNx:H is applied as antireflection coating.

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