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## THE EFFECT OF VOID FORMATION ON THE RELIABILITY OF ED-XRF MEASUREMENTS IN LEAD-FREE REFLOW SOLDERING

## WPLYW POWSTAWANIA PUSTEK NA WIARYGODNOŚĆ BADAŃ ED-XRF BEZOŁOWIOWYCH ZŁĄCZY LUTOWANYCH ROZPLYWOWO

In lead-free reflow soldering, the presence of voids should be taken into account. For this reason, the effect of the applied heating profiles was examined via the characterization of voids in galvanic and immersion Sn coatings. According to EU Directive 2002/95/EC, the screening of Pb element of reflow soldering (i.e. of electrical and electronic equipment) is necessary; and the practical implementation of this measurement is largely affected by the characteristics of the solder (i.e. the presence of voids and the inhomogeneity of the solder). Comparing the results of the above two coating methods, it was found that by chemical coating more voids were formed and the detected lead content was higher than for galvanic Sn. The standard deviation of Ag and Cu concentrations was mainly influenced by the appearance of large compounds in the second case, while with chemical coating, no large compounds were formed due to the elevated number of voids.

*Keywords:* ED-XRF, lead-free, void, intermetallic, reflow

### 1. Introduction

Due to the advanced productivity of the technology, reflow soldering (i.e. Surface Mounted Technology) is of importance to the electronic industry. The applicability of SMT depends primarily on the size of the parts to be processed, but the alternative Pin-in-Paste Technology for wired bonds (originally called Through Hole Technology) is also applied. Reflow soldering technology includes three main steps: paste printing (a mixture of solder powder and flux), stepwise mounting and a final melting (reflow) step. Throughout the process, the characteristics of the paste [1, 2] have an effect on the heating profile [3, 4], and thus, partly determine the temperature range (including the optimal profile). The most reliable soldering bond is the outcome of an optimized temperature profile.

During the lead-free soldering process, the formation of voids is common. Unfortunately, voids significantly reduce the reliability of soldering bonds [5], partly because large voids decrease useful cross-sections. The main parameters and mechanisms of void formation are well-known [6], e.g. surface preparation has an influence on wettability, which relates to the formation of voids [7]. 2D X-ray inspection is a useful tool for the characterization of voids in soldering bonds, e.g. for the credible identification of 5-10 micron-sized voids [8]. Generally, the size, the count number and the area fraction of voids are examined in soldering bonds [8, 9], but we have also found a study on the position of voids in BGA solder balls [5].

According to EU Directive 2002/95/EC (on the Restriction of Hazardous Substances), lead-free bonds should contain less than 0.1 wt% Pb element [10]. In the electronics industry, the level of contaminants is usually determined by using non-destructive ED-XRF (Energy Dispersive X-Ray Fluorescence) method. Nowadays, portable devices are widely used [11, 12]; however, the use of desktop equipment is preferred because it ensures better repeatability [13] and allows the use of higher excitation voltage. During XRF examination, the analysed samples must have flat surfaces, since this is the only way that the method provides correct results. The test is usually based on pure element calibration method (i.e. Fundamental Parameter method) [14-16], which allows for performing standard-free measurements by using spectral library.

### 2. Experimental procedure

Twelve pieces (6 galvanic and 6 immersion) of printed circuit boards (PCB) were investigated. Each PCB had 10 pads with 4×5 mm<sup>2</sup> tinned surface of 1 μm thickness. The samples were prepared by paste printing (95.5wt%Sn-4wt%Ag-0.5wt%Cu alloy powder mixture with 10% flux), and a heating process (TABLE 1) was applied. The thickness of the print deposition was about 150 μm, which provided an infinitely thick layer for XRF analysis. The temperatures of the experimental heating profiles can be seen in TABLE 1 where preheating zones (1-5) have the same val-

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ues for all cases for the best activation of flux. The temperatures of the peak zones ( $T_{PEAK}$ , 6-7) were set at three different levels (low, normal, high), including extreme cases. The transportation speed in the reflow oven was kept constant (800 mm/minute).

TABLE 1

Temperatures of the reflow oven\*

Heating Profile	Zone Temperatures [°C]					$T_{PEAK}$ : 6,7
	1	2	3	4	5	
Low	130	150	177	197	225	$LT_{PEAK}$ : 230, 230
Normal	130	150	177	197	225	$NT_{PEAK}$ : 250, 260
High	130	150	177	197	225	$HT_{PEAK}$ : 275, 280

\* $N_2$  inert gas atmosphere was applied

The XRF measurements were performed with a Fischerscope X-ray XDAL spectrometer operating at 50 kV. The X-ray fluorescence spectra were collected with a silicon PIN detector of high energy resolution (<200 eV). The samples were measured for 180 s using a mid-size collimator (0.6 mm). Computation by WinFTM (Windows-based) v.6.20 software [17] was based on the fundamental parameter method.

Phoenix PCBA 2D X-Ray equipment with Vintage software was used for 2D X-Ray measurements. After the 2D analysis, an image processing of X-Ray photos was performed with Leica QWin Pro 2.3 and Cprob software.

The measurements were carried out directly on the reflow soldering bonds. The XRF measurements were carried out at 10 points for each temperature profile, while with the 2D X-ray technique, 5 randomly selected soldering bonds were examined per profile.

Observations on the cross-sectional microstructures were made using an AMRAY 1830I type Scanning Electron Microscope. 2% of Nital (2%  $HNO_3$ + 98% isopropanol) was used to etch the microstructures.

### 3. Results and discussion

The measured concentrations at galvanic Sn in Fig. 1 show that the amount of Cu is twice as large for the normal

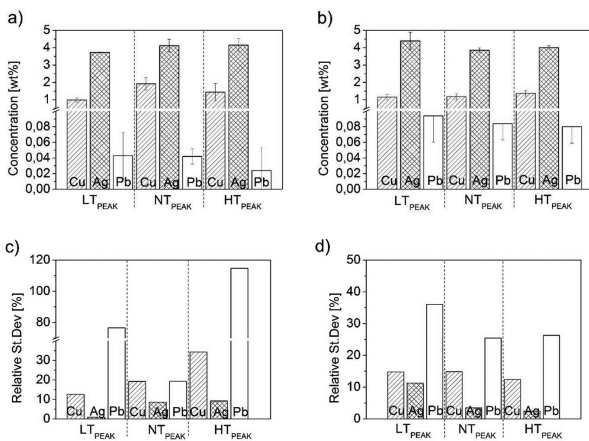


Fig. 1. Measured concentrations of Cu; Ag and Pb elements at galvanic Sn (a; c) and immersion Sn (b; d),  $LT_{PEAK}$  = Low  $T_{PEAK}$ ,  $NT_{PEAK}$  = Normal  $T_{PEAK}$ ,  $HT_{PEAK}$  = High  $T_{PEAK}$

case ( $1.92 \pm 0.51$  wt %) as that for the low case ( $0.99 \pm 0.17$  wt %), which means that increased Cu dissolution occurred in the PCB pad. In the case of immersion coated samples, there were no significant differences in Cu dissolution. However, the lowest Cu concentration was detected at low temperature (Low  $T_{PEAK}$ ) for both types of coating.

Using the same paste, other considerable differences occurred: the lead concentration was nearly twice as high in immersion coated as that in galvanic samples. Increased temperature resulted in lower lead content for both cases. It is important to note, that the detected Pb content in immersion coated samples by far exceeded the rule of the RoHS specification ( $700-3\sigma$ , ppm), which calls for the use of a more sensitive analytical tool, such as ICP-OES [10]. The possible reasons for the differences in Pb concentration were examined by analysing the texture and the voids/by texture and void analysis.

The relative standard deviation (RSD, %) values of Cu and Pb elements were above 10%. The RSD value of Cu increased with temperature at galvanic Sn. In those cases where Cu dissolution exceeded the threshold value [18], large  $Cu_6Sn_5$  IMCs (of about 30-50  $\mu m$ ) were occasionally formed in the bulk solder (Fig. 2) at random positions. It is important to note that large IMCs and the dispersion of these phases cause poor reliability of the bonds [6, 7]. IMCs of size 1-5  $\mu m$  were found in the bulk solder in the normal case. IMC layers were also observed in the cross-sectional images. The thicknesses were  $3.2 \pm 0.5 \mu m$ ,  $5.1 \pm 1.0 \mu m$  and  $6.7 \pm 1.6 \mu m$  from low to high  $T_{PEAK}$  for galvanic Sn and  $2.7 \pm 0.9 \mu m$ ,  $4.2 \pm 0.3 \mu m$  and  $5.9 \pm 0.4 \mu m$  for immersion Sn, respectively.

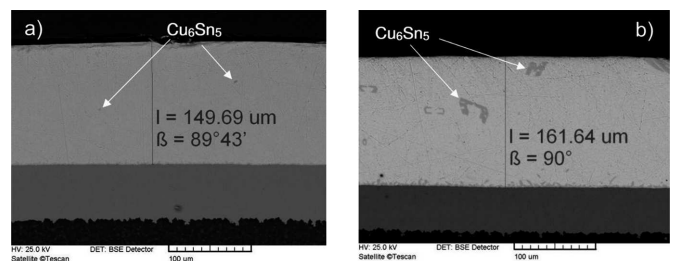


Fig. 2. IMCs in bulk solders; (a)  $>10 \mu m$   $Cu_6Sn_5$  phases at  $LT_{PEAK}$ ; (b)  $\sim 30-50 \mu m$   $Cu_6Sn_5$  phases at  $HT_{PEAK}$

There were no significant differences between the maximum diameters of the voids in galvanic Sn ( $22 \pm 3 \mu m$ ;  $25 \pm 3 \mu m$  and  $24 \pm 3 \mu m$ , from low to high  $T_{PEAK}$ ), but it was found that the area ( $3.0 \pm 0.3\%$ ;  $1.9 \pm 0.2\%$ ;  $1.1 \pm 0.2\%$ ) and the count number ( $97 \pm 20$  pcs;  $45 \pm 3$  pcs;  $37 \pm 11$  pcs) of the voids strongly depended on the temperature. In the case of normal  $T_{PEAK}$  profile, the measurement uncertainty for Pb was small due to the most homogeneous microstructure of the bulk solder. In contrast to that, hundreds of voids ( $272 \pm 22$  pcs;  $297 \pm 79$  pcs;  $350 \pm 63$  pcs) were formed in immersion coated samples, where the area fraction ( $4.3 \pm 0.4\%$ ;  $5.6 \pm 0.7\%$ ;  $7.6 \pm 0.6\%$ ) and the maximal size of the voids ( $25 \pm 3 \mu m$ ;  $27 \pm 3 \mu m$  and  $28 \pm 2 \mu m$ ) also increased.

Based on the studies of void formation in Sn-Ag-Cu solder alloys on Cu substrate [2, 5], it can be concluded that the characterization of voids is not negligible. By applying image analysis, the count and the area parameters were determined (Fig. 3). Grey images were transformed into binary

images using greyscale levels (the segregation of voids from the background) and then the detected objects were measured. The number of dilation operator (NoD) was also applied (TABLE 2) to characterize the distribution of voids (Fig. 4).

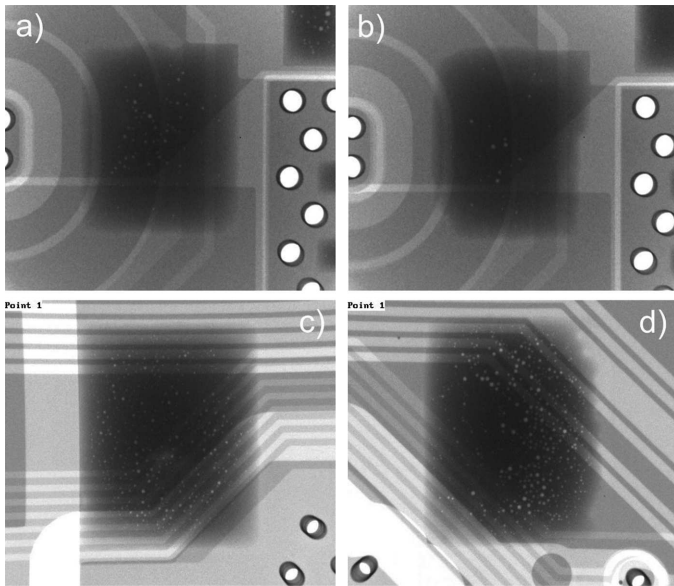


Fig. 3. Characteristics of voids [area fraction; count number; maximum diameter] in bulk solders for cases of galvanic Sn (a; b) and immersion Sn (c; d); (a)  $LT_{PEAK}$  [2.4%, 69 pcs,  $d_{max} = 22 \mu m$ ]; (b)  $HT_{PEAK}$  [1.3%, 30 pcs,  $d_{max} = 22 \mu m$ ]; (c)  $LT_{PEAK}$  [4.6%, 255 pcs,  $d_{max} = 24 \mu m$ ]; (d)  $HT_{PEAK}$  [7.1%, 333 pcs,  $d_{max} = 28 \mu m$ ]

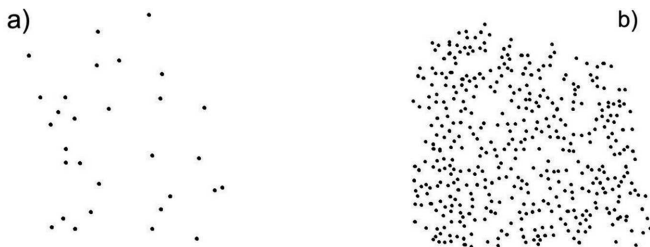


Fig. 4. Examples for the distribution of voids in bulk solders at High  $T_{PEAK}$  (in binary images); (a) galvanic Sn; (b) immersion Sn

TABLE 2

The results of the image analysis process

		Low Profile		Normal Profile		High Profile	
		galv. Sn	imm. Sn	galv. Sn	imm. Sn	galv. Sn	imm. Sn
Void [pcs]	Average	97	272	45	297	37	350
	St.Dev.	14	36	2	57	8	46
	RSD [%]	15	13	5	19	21	13
NoD [pcs]	Average	39	36	40	22	51	18
	St.Dev.	20	27	18	9	12	4
	RSD [%]	50	75	46	42	23	23

The distribution of voids was analysed by making a comparison with reference pictures published by Ghosh et al. [19]. It can be concluded, that the voids were not clustered. Highlighting the random distribution of the voids is very important;

in this way, only the number of voids will make a difference during XRF analysis.

Based on the data shown in TABLE 2, it can be stated, that the number of dilatation greatly depends on the number of voids. It can be observed that the standard deviation (and also the RSD) of NoD values decreases with increasing temperature, i.e. smaller differences occur in the deviation of voids at higher temperatures. The applied changes in temperature contrarily affect the number of voids in both coatings.

#### 4. Conclusion

The prepared PCB samples were reflowed using three different time-temperature profiles, and examined with ED-XRF and 2D X-Ray techniques after the heat treatment. Based on the results, it can be stated, that the growing number of inclusions results in rising the (measured) Pb-content, while the growth (and random position) of compound phases increases the uncertainty of the measured Pb-content. In addition, the substantial deviation in Cu values indicates the presence of large dimensional compound phases. Considering the surface preparation process, much more cavities were formed in immersion Sn coated samples than in galvanic coated ones, while large dimensional compound phases appeared mainly in the case of galvanic coating (at high-temperature profile).

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#### REFERENCES

- [1] N-C. Lee, Reflow Soldering Processes and Troubleshooting: SMT, BGA, CSP and Flip Chip Technologies, Oxford 2002.
- [2] M.R. Harrison, J.H. Vincent, H.A.H. Steen, Sold. & Surf. M. Tech., **13**, 3 (2001).
- [3] K.J. Puttlitz, K.A. Stalter, Handbook of Lead-Free Solder Technology for Microelectronic Assemblies, New York 2004.
- [4] E.H. Amalu, W.K. Lau, N.N. Ekere, R.S. Bhatti, S. Mallik, K.C. Otiaba, G. Takyi, J. Microel. Eng. **88** (2011).
- [5] M. Yunus, K. Srihari, J.M. Pitarresi, A. Primavera, J. Microel. Rel. **43** (2003).
- [6] D. Shangguan, Lead-Free Solder Interconnect Reliability, USA 2005.
- [7] K. Zeng, K.N. Tu, J. Mater. Sci. Eng. R **38** (2002).
- [8] A. Sharif, Y.C. Chan, R.A. Islam, Mat. Sci. and Eng. B **106** (2004).
- [9] M.A. Dudek, L. Hunter, S. Kranz, J.J. Williams, S.H. Lau, N. Chawla, J. Mat. Char. **61**, 4 (2010).
- [10] P. Cusack, T. Perrett, J. Plast., Addit. and Comp. **8**, 3 (2006).
- [11] S. Biligiri, J. Met. Finish. **105**, 4 (2007).
- [12] F. Reilly, J. Met. Finish. **105**, 10 (2007).

- [13] R.P. Alvarez, A. Markowicz, D. Wegrzynek, E.C. Cano, S.A. Bamford, D.H. Torres, J. X-Ray Spectr. **36** (2007).
- [14] J. Sherman, J. Spectrochim. Acta **7** (1955).
- [15] G.R. Lachance, R.J. Traill, Canadian J. Spect. **11** (1966).
- [16] M. Bos, J.A.M. Vrielink, J. Anal.Chim.Acta **373** (1998).
- [17] V. Rößiger, B. Nensel, Analyse von Schichtdicken mit Röntgenfluoreszenz, Jahrbuch Oberflächentechnik, Bad Saulgau 2004.
- [18] C.K.S. Alex, Y.C. Chan, IEEE Trans. on Comp., Pack., and Man. Tech. **B 19**, 3 (1996).
- [19] S. Ghosh, Z. Nowak, K. Lee, J.Acta Mater. **45**, 6 (1997).

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